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A SWITCHED-CAPACITOR PHASE-LOCKED LOOP

by

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March 1987

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A Switched-Capacitor Phase-Locked Loop

by

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requirements for the degree of

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ABSTRACT

In this research the thesis objective was to replace the resistors of an RC network resulting in a sampled data equivalent network. The switched capacitor resistors are exactly equivalent to resistors by themselves; however, such an equivalence may not hold true when the realizations are used to replace resistors of an RC active network. During the research, firstly, the types of replacement methods and their properties were discussed. Furthermore, the main SC building blocks were presented and a second order switched-capacitor phase-locked loop was implemented in hardware.

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I dedicate this thesis to my father-in-law.

I also would like to express my gratitude to Professor Sherif Michael for all his teaching and understanding, and to my wife for all her understanding and help.

I. INTRODUCTION

A. THE NEED FOR SWITCHED CAPACITOR REALIZATION

The periodic sampling of analog signals has been used for many years to implement basic analog signal processing functions. These functions include amplifiers, summers, delays, sample-and-hold, integration, and differentiation. One of the primary advantages of these circuits is that they provide an economic and accurate implementation of analog circuit functions with existing integrated circuit technology.

Continuous analog circuits are composed of resistors, capacitors, and active devices. However, the performance of these circuits depends upon the accuracy of the resistors and capacitors. Especially in filters, this becomes a serious problem because the RC product must be accurately defined for a desired performance. To obtain a sufficient absolute value accuracy most of the circuits designed using these elements need external trimming. Another serious problem is the changes in the values of the passive components as temperature changes. Resistor and capacitor values may not change by the same amount and the same direction, which may pose a serious problem in some critical situations. Besides these undesirable properties, large values of time constants require large values of resistance which also requires large areas in the integrated circuit.

Analog sampled data techniques provide a unique solution to the above problems. It will be shown that the resistor can be replaced by switches and capacitors. Filters using switched-capacitor (SC) techniques overcome a major obstacle to filter-on-a-chip fabrication, by simulating resistors with high-speed switched capacitors. Such an approach thus eliminates the necessity for precise integrated resistor values that require costly trimming procedures and permits fabrication of precise monolithic analog capacitor filters. This results in the important fact that the circuit performance and the accuracy is determined by capacitor ratios. Ratios of elements are always easier to control. MOS IC technology can implement capacitor ratios to within about 0.3% of specified values, [Ref. 1]. Since the only concern is the ratios rather than individual values of capacitors, it can be possible to use very small capacitance values in the integrated circuit, resulting in smaller chip areas.

The advantage of the switched capacitor realization of resistors can be appreciated by comparing the RC time constant, τ, of a resistor R_1 and a capacitor C_2, as

$$\tau = R_1 C_2 \tag{1.1}$$

If a larger time constant is required, R or C or both can be made large, resulting in a larger chip area. When the resistor is replaced with a SC realization, Equation 1.1 becomes

$$\tau = T_c \frac{C_2}{C_1} \tag{1.2}$$

where T_c is the clock period and C_1 is the capacitor used by the SC realization, assuming that R_1 is replaced by a series or parellel SC equivalent. In this case larger time constants can be obtained by increasing the capacitor ratios rather than increasing the individual capacitor values, resulting in a smaller chip area.

Another concern is to maintain the time constant accuracy. If the accuracy is defined as $d\tau / \tau$ for τ, the following expression can be written

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \tag{1.3}$$

where dR_1 / R_1 represents the resistor accuracy and dC_2 / C_2 represents the capacitor accuracy. The worst case accuracy of τ will be the sum of the absolute accuracies of R_1 and C_2, which is very poor if R_1 and C_2 are implemented on an integrated circuit. If the SC equivalent of R_1 is used, the accuracy of τ can be expressed as

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \tag{1.4}$$

Assuming that T_c is perfectly accurate, that is, $dT_c / T_c = 0$,

$$\frac{d\tau}{\tau} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \qquad (1.5)$$

Because the two capacitors C_1 and C_2 are built close together, using the same technology, the acuracy of Equation 1.3 is much improved over that given in Equation 1.5. Furthermore, because the capacitors are similar in many respects, such properties as linearity and temperature coefficients are well behaved. When the temperature changes, their values change by the same amount toward the same direction, leaving the ratio almost constant. This is indeed a very satisfying result when τ must be carefully controlled.

B. SWITCHED CAPACITOR EQUIVALENT RESISTORS

A Switched-capacitor consists basically of a capacitor whose charge is transferred from one node to another by a switch, thus simulating a resistor.

The switched capacitor resistor of Figure 1.1 (a) is called the parallel switched capacitor resistor realization. It simulates the circuit of Figure 1.1(b). The switch symbol will always be drawn open. It will be assumed that the switches are controlled by the application of a two-phase clock. The period of time is divided into two equal segments as illustrated in Figure 1.1 (c). The segments will be called phase periods. It will be assumed that the phase periods are seperated by a finite period of time in which all the switches are open. This situation is called nonoverlapping clocks, which is a very important property for switched capacitor networks. The open-closed positions of the switches will be determined by the phases of the clock, the switch is closed when the waveform is high and open when the waveform is low.

It can be consider that the analog sampled data realizations correspond to one topology during the Φ_2 (or Φ_1) clock phase and to a second topology during the Φ_1 (or Φ_2) clock. A useful complementary notation for the clock phases is denoted by even and odd, which can be associated to Φ_2 and Φ_1 by definition. In fact, practically, to ensure that the even and odd switches are never turned on simultaneously, the clocks are made nonoverlapping (i.e., the duty cycle is slightly less than 50%). It is noted that turning both the Φ_e and Φ_o switches off simultaneously does not affect the behavior of the circuit.

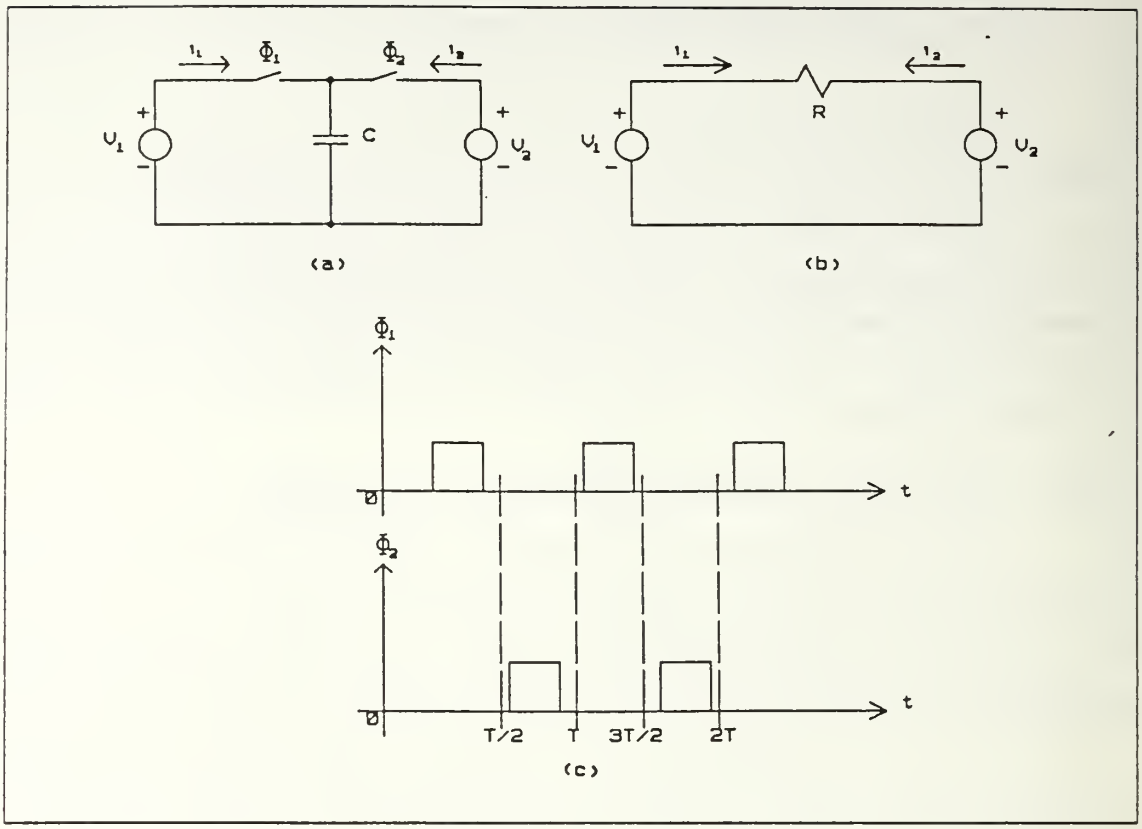

Figure 1.1 Parallel Switched Capacitor Realization.
(a) Switched capacitor realization of a continuous resistor. (b) Continuous resistor.
(c) Clock waveforms for the switched capacitor realization.

Both input and output of the SC network are sampled data signals which change in value only at the switching instants kT. Thus, the voltage sources and internal circuit voltages are assumed to be sampled at times kT and held over a one-half clock period interval, T. To illustrate graphically, the sampled-data voltage waveform in Figure 1.2 (a) can be partitioned into its even and odd components as shown, respectively, in Figure 1.2 (b) and (c).

Mathematically it can be expressed as

$$v(t) = v_o(t) + v_e(t) \tag{1.6}$$

or in the z-domain

$$V(z) = V_o(z) + V_e(z) \tag{1.7}$$

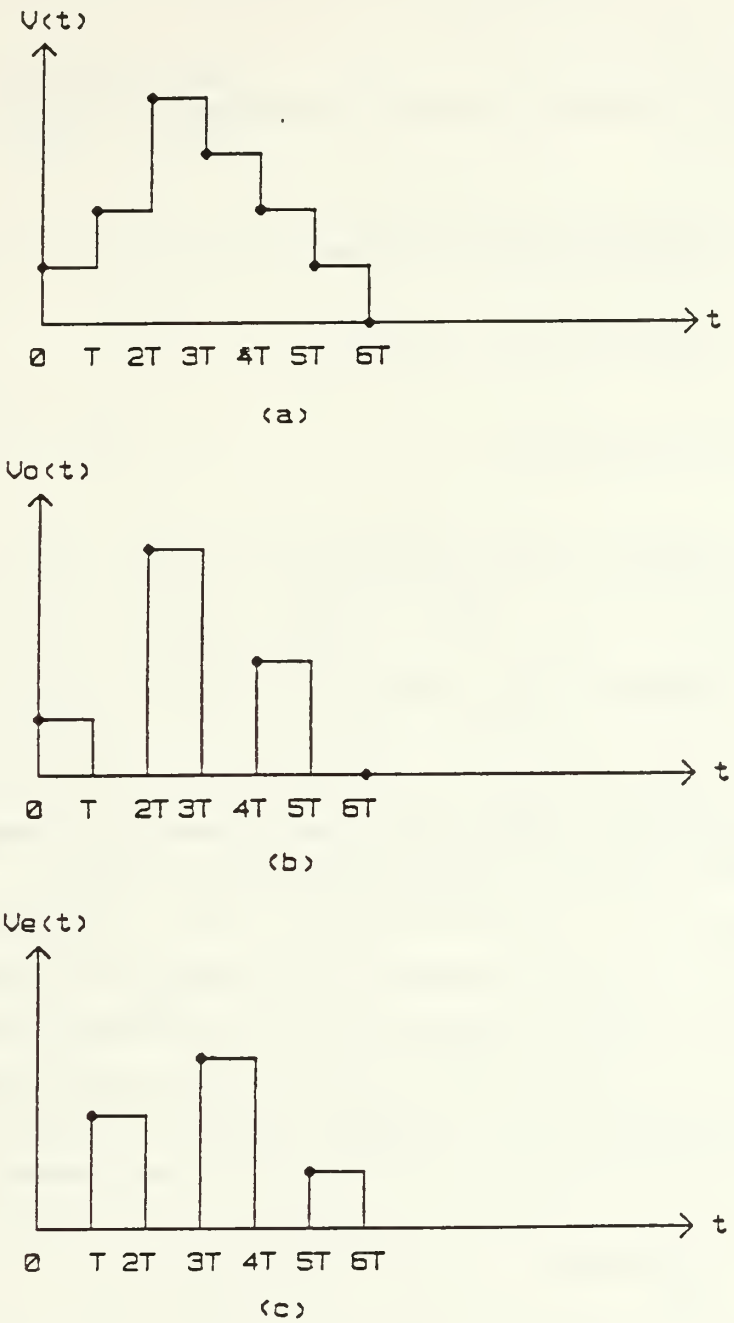

Figure 1.2 (a) Sampled Data Voltage Waveforms Partitioned into (b) Even and (c) Odd Components.

where

$$V_o(z) = z^{-1\ 2}V_e(z) \tag{1.8}$$

The input and output voltages of a time-varying sampled data network can be expressed as

$$V_{in}(z) = V_{in}{}^{o}(z) + V_{in}{}^{e}(z) \tag{1.9}$$

$$V_o(z) = V_o{}^{o}(z) + V_o{}^{e}(z) \tag{1.10}$$

This can be made equivalent to

$$V_{in}(z) = V_{in}(z)|_{\Phi_1} + V_{in}(z)|_{\Phi_2} \tag{1.11}$$

$$V_o(z) = V_o(z)|_{\Phi_1} + V_o(z)|_{\Phi_2} \tag{1.12}$$

Therefore, at least four transfer functions are possible if $V_o(z)$ is sampled at all times, then the effects during Φ_1 and Φ_2 clock phases must be added.

The charge of the capacitor in Figure 1.1 (a) is transferred from one node to another using the switches controlled by the two-phase clock. The first clock pulse, Φ_1, which will occur during the first phase period, will close switch 1. At this time, C will be charged to V_1. In practice, a finite resistance R is associated with the switch, that is, C cannot be charged to V_1 in zero time. Obviously, the RC time constant must be much less than the width of Φ_1 for the charge, Q_1, to be transferred

$$Q_1 = CV_1 \tag{1.13}$$

The second clock pulse, Φ_2, which will occur during the second phase period, will close switch 2. At this time, C will be discharged to

$$Q_2 = CV_2 \tag{1.14}$$

An amount of charge equal to $\Delta Q = Q_1 - Q_2$ is transfered from one terminal to another. This charge transfer represents an equivalent current of

$$I = \frac{\Delta Q}{T} = \frac{V_1 - V_2}{\frac{1}{C}T} \tag{1.15}$$

and the form of this equation indicates that the switched capacitor can be modeled as a resistor of value

$$R_{eq} = \frac{1}{f_c C} \tag{1.16}$$

where $f_c = 1/T$ is the switching frequency in Hertz. The switched capacitor resistor of Figure 1.1 (a) is called the parallel switched capacitor resistor realization, [Ref. 2].

A second switched capacitor realization of the continuous resistor is given in Figure 1.3. This configuration is called the series switched capacitor resistor realization of the continuous resistor.

In the series case, V_1 is connected to V_2 through C for a portion of the clock period, the second phase period. The first clock phase makes the capacitor short circuit, therefore, Figure 1.3 is valid only at Φ_2.

$$Q_1 = 0$$
$$Q_2 = C(V_2 - V_1)$$
$$\Delta Q = Q_1 - Q_2$$
$$\Delta Q = C(V_1 - V_2)$$

Using the above equations, we find Equation 1.15 and Equation 1.16 again for the series switched-capacitor case.

A third realization is a combination of the parallel and series configuration and is shown in Figure 1.4. This configuration is called the series-parallel realization of a resistor. The circuit can be analyzed by using similar technique as for the previous two realizations. At Φ_1 or $t = T/2$, the charge which flowed across the left dotted line in the direction of i_1 is shown in Figure 1.5 (a). This charge is

$$Q_1(T/2) = C_2 V_1 \tag{1.17}$$

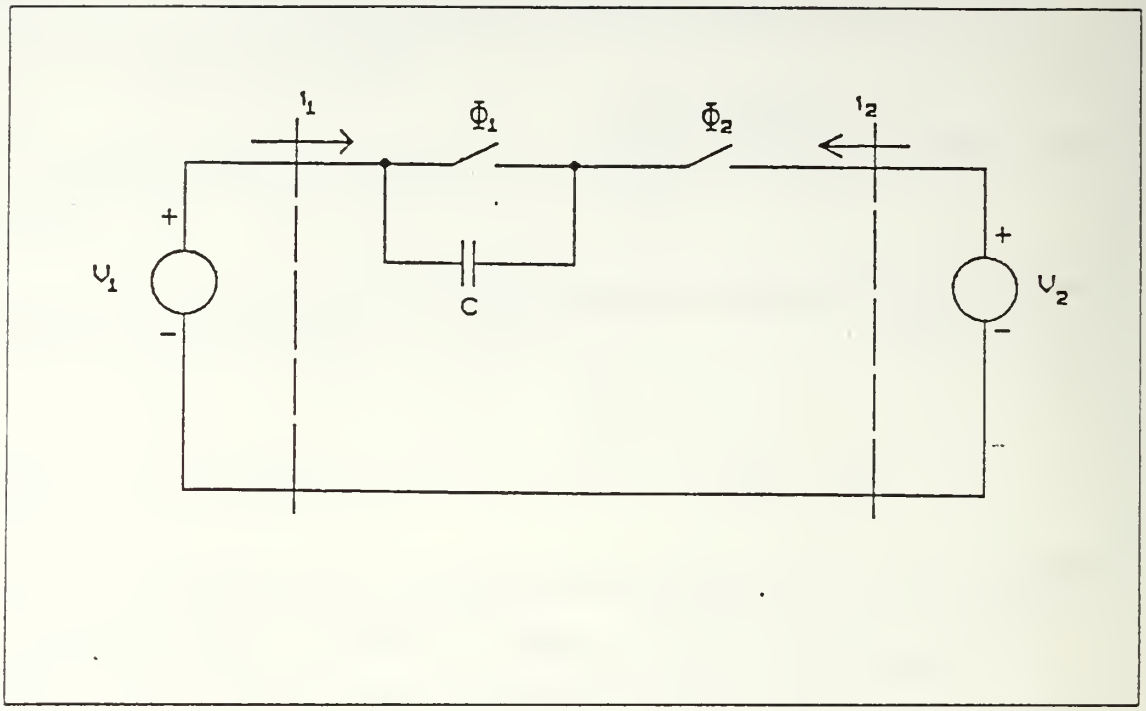

Figure 1.3 Series Switched Capacitor Realization of a Continuous Resistance.

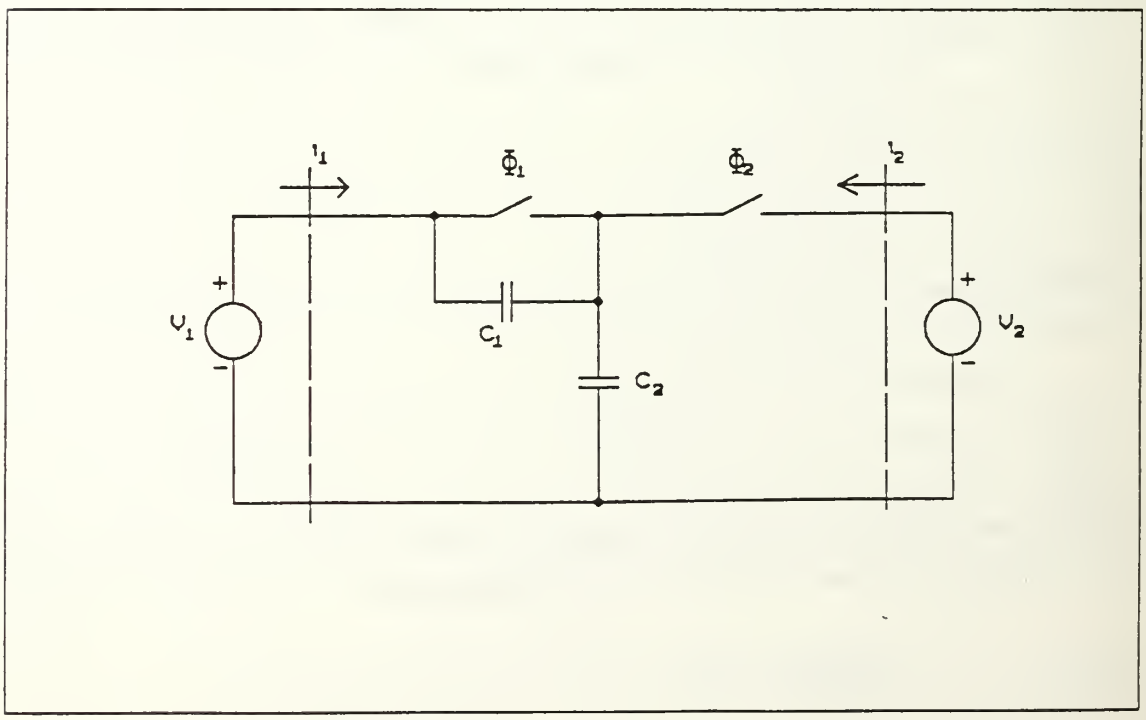

Figure 1.4 Series-Parallel Switched Capacitor Realization of a Continuous Resistance.

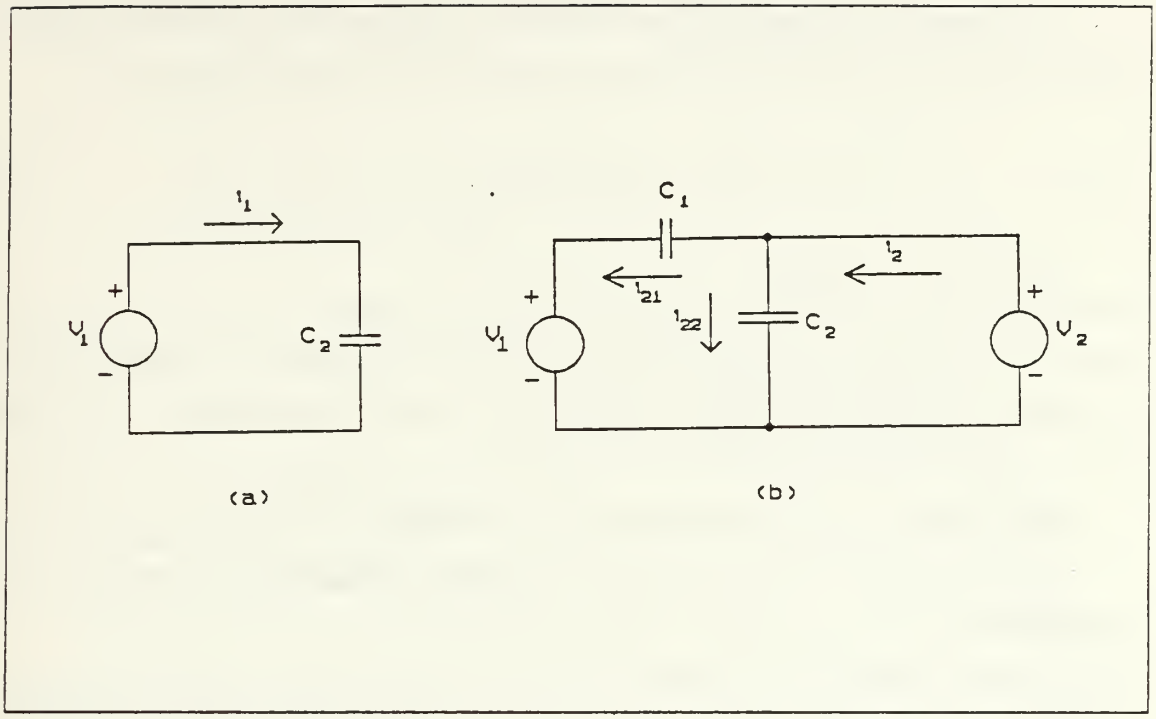

Figure 1.5 Series-Parallel Switched Capacitor Realization.
(a) Φ_1, first phase period (b) Φ_2, second phase period.

At Φ_2 or t = T, the charge which flowed across the right dotted line in the direction of i_2 is

$$\begin{aligned} i_2 &= i_{21} + i_{22} \\ Q_2(T) &= C_1(V_2-V_1)+C_2V_2 \end{aligned} \tag{1.18}$$

An amount of charge equal to $\Delta Q = Q_1 - Q_2$ transfered from one terminal to another. This charge transfer also represents an equivalent current, I;

$$\begin{aligned} \Delta Q &= C_2V_1-C_1V_2+C_1V_1-C_2V_2 \\ &= (V_1-V_2)(C_1+C_2) \end{aligned}$$

$$I = \frac{\Delta Q}{T}\,\frac{(V_1-V_2)}{\dfrac{1}{C_1+C_2}T} \tag{1.19}$$

and the form of this equation indicates that this type of realization can also be modeled as a resistor of value

$$R_{eq} = \frac{T}{C_1 + C_2} = \frac{1}{(C_1 + C_2)f_c} \tag{1.20}$$

if $C_1 = C_2 = C$, then;

$$R_{eq} = \frac{1}{2Cf_c} \tag{1.21}$$

when Equation 1.16 and Equation 1.21 are compared, it can be seen that the series-parallel realization may result half the equivalent resistance value for the same clock frequency.

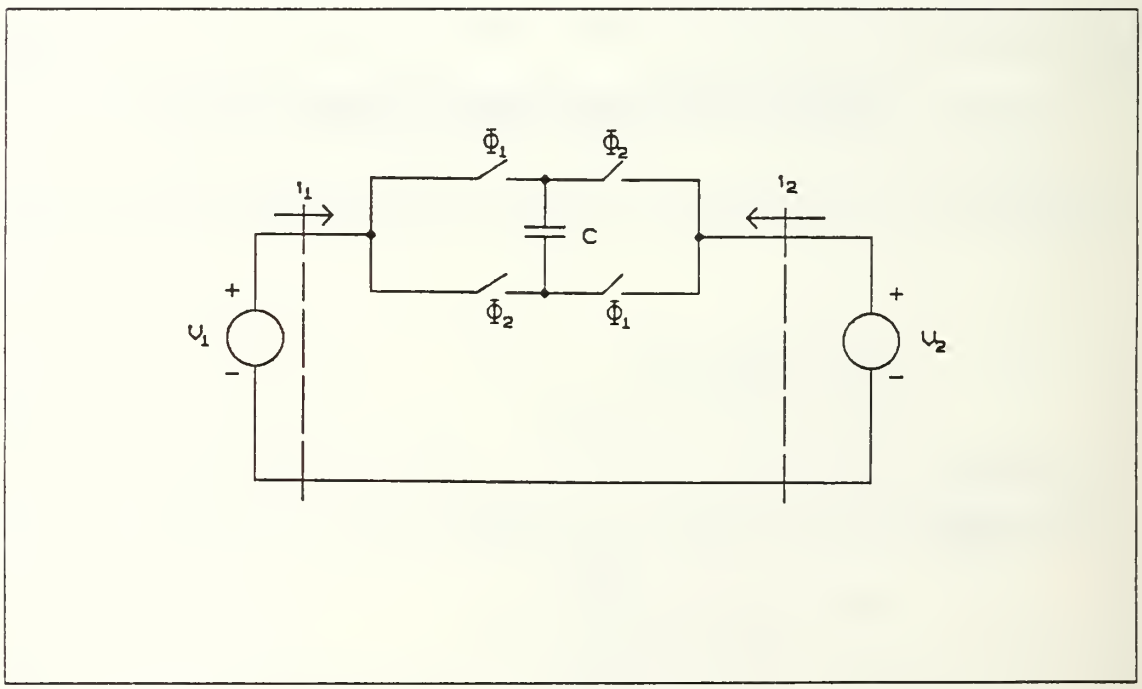

Figure 1.6 Bilinear Switched Capacitor Realization of a Continuous Resistance.

A fourth switched capacitor resistor realization is shown in Figure 1.6 This configuration is called the bilinear switched capacitance realization of a resistor. In the

bilinear SC resistor realization, a complete clock period is really T/2 rather than T, because the input signal waveform is sampled twice in a single clock period.

It can be shown that this realization results in an equivalent resistor given below.

$$R_{eq} = \frac{T}{4C} = \frac{1}{4Cf_c} . \tag{1.22}$$

Although the bilinear realization has basically the same performance as the series-parallel realization, there are some practical differences that are important. When each of the above realizations is replaced by the resistors in an analog network, resulting in a switched capacitor network, each will be found to possess different properties. This will be shown in the following chapter.

C. PHASE LOCKED LOOP (PLL)

A phase-locked loop is a device by means of which the phase of a frequency-modulated oscillator output signal is forced to follow the input signal. A diagram of this device is shown in Figure 1.7.

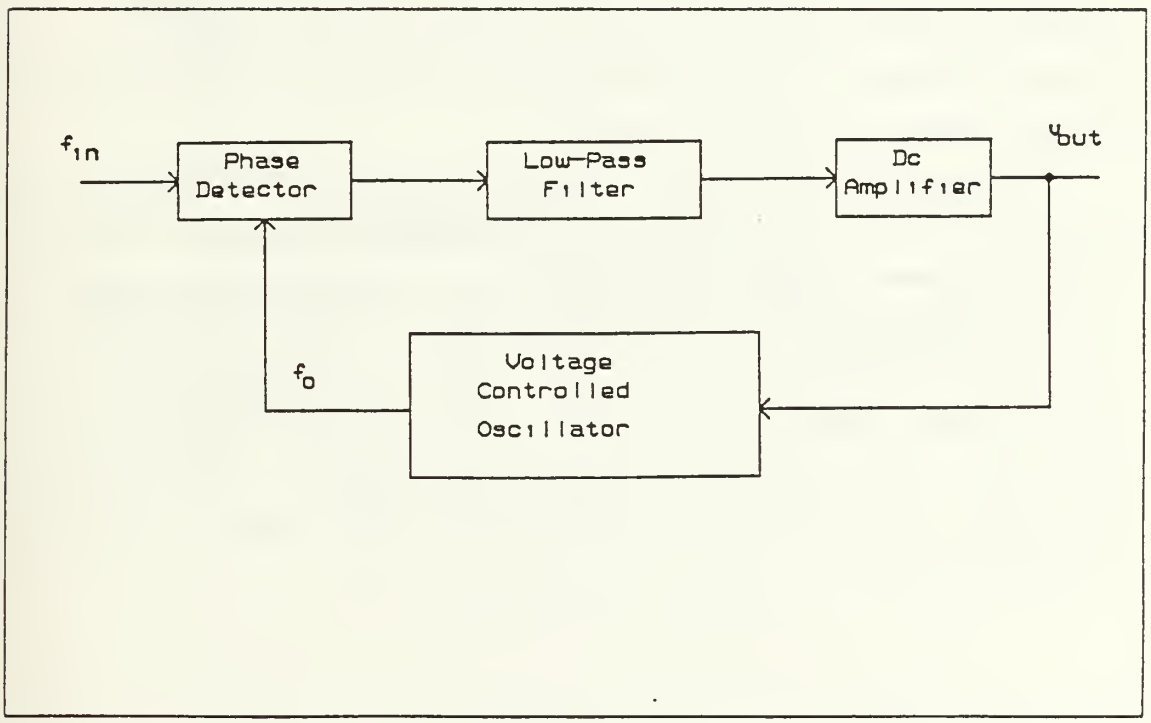

Figure 1.7 Phase Locked Loop System, (PLL).

The input to the PLL circuit is a frequency, not a dc voltage, and the circuit operates in the following manner:

1. The incoming frequency is one input to the phase detector.
2. The output from the VCO, also a frequency, is the second input to the phase detector.
3. The output of the phase detector is a function of the phase difference between the two signals applied. This error voltage, after low-pass filtering in the loop filter and amplifying by the dc amplifier, is applied to the modulation input of the voltage controlled oscillater (VCO).
4. This dc signal voltage causes the VCO to begin varying its frequency in the direction of the incoming frequency. When the loop is in lock, the two signals to the comparator are of the same frequency although not necessarily in phase. A fixed phase difference between the two signals to the phase detector results in a fixed dc voltage to the VCO. Changes in the input signal frequency then result in change in the dc voltage to the VCO.

The VCO can operate over different frequency ranges through the selection of different RC time constants. The VCO in a phase-locked loop has a "free-running" or "center" frequency (f_o), which is the frequency of the VCO when not locked to the incoming signal frequency. As the incoming frequency approaches the free running frequency of the VCO, the output of the phase detector begins forcing the frequency of the VCO toward a lock condition. The range over which this action occurs is called the "capture" or "lock-in" range. The "lock", "tracking", or "hold-in" range is the range of incoming signal frequencies over which the loop will remain locked. The capture range is always smaller than the lock range. Figure 1.8 shows the relationship between the capture range and the lock range, [Ref. 3].

It can be seen from Figure 1.8 that as an incoming signal frequency increases toward the free-running frequency, the loop will capture the signal at a frequency close to the free-running frequency and then lose lock at a frequency on the other side of the free-running frequency further away. The frequency at which the PLL loses lock is the end of the lock range, and this is always a broader range than the capture range. As a higher frequency signal decreases relative to the free-running frequency, the previous operation is repeated in a reverse manner. Both the capture and the lock ranges are determined by the cutoff frequency of the low-pass filter which also determines the bandwith of the PLL.

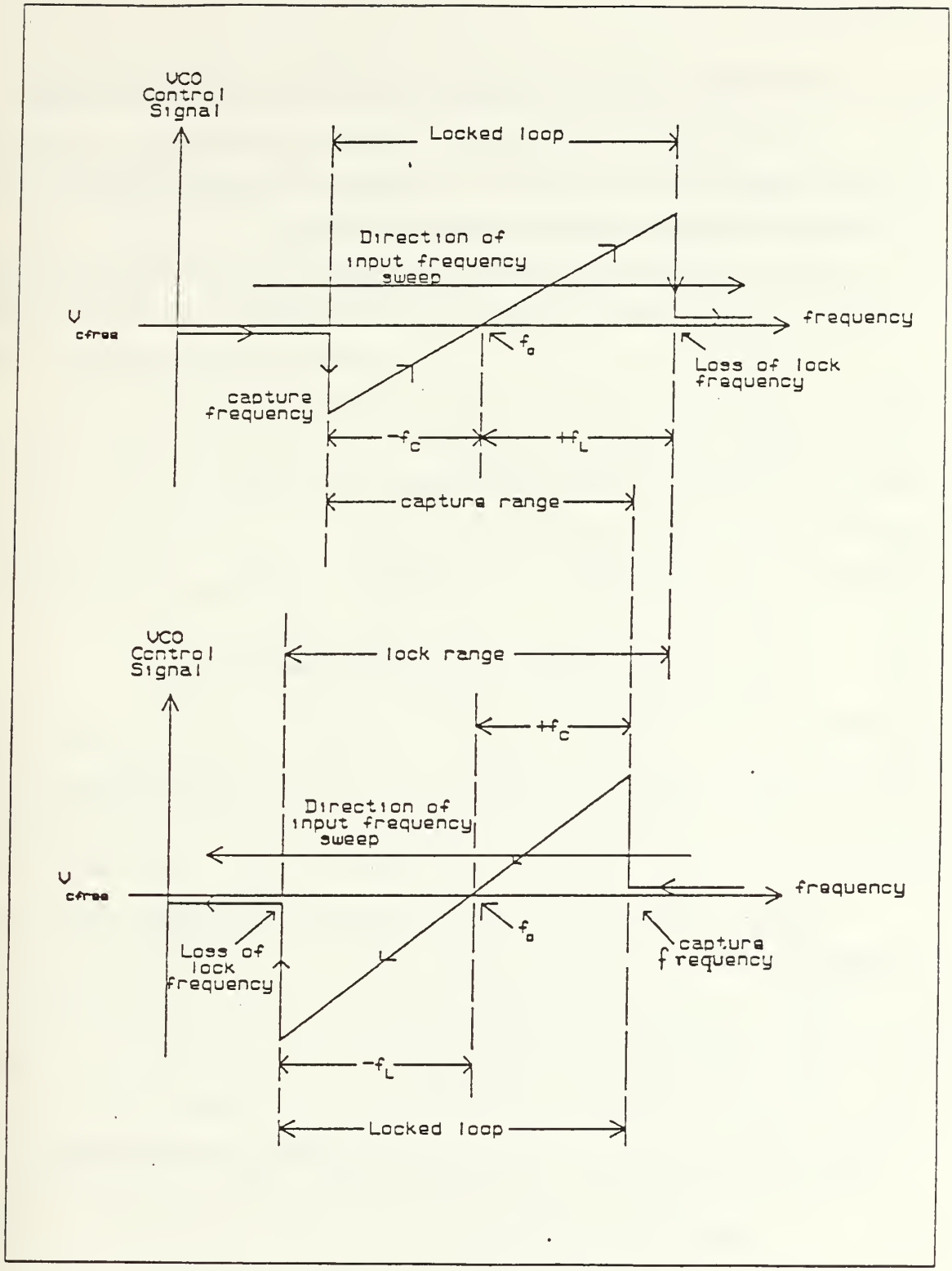

Figure 1.8 Capture and Lock Range of the PLL.

II. SWITCHED CAPACITOR EQUIVALENT RC NETWORKS

In this chapter, the main goal will be developing realizations for continuous RC passive networks. The realizations of such networks are done by the replacement of the continuous realizations developed in the previous section.

As an example an RC passive low-pass filter will be realized using switched capacitor equivalent resistance technique, resulting an analog sampled data realization.

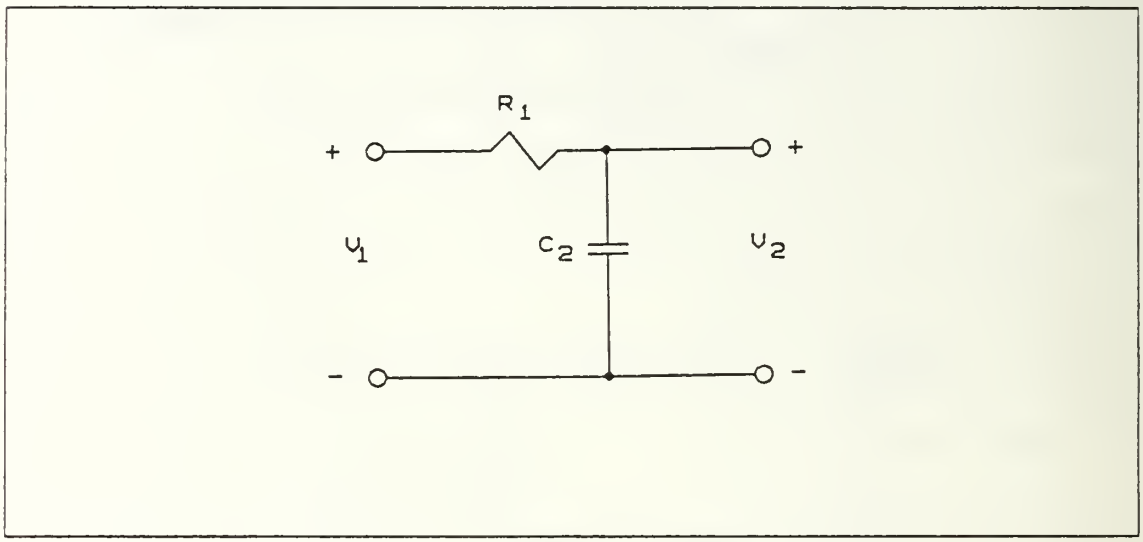

Figure 2.1 Continuous RC Circuit.

In Figure 2.1 the continuous frequency domain transfer function of this circuit is given as

$$H(s) = \frac{1}{s\tau_1 + 1} = \frac{1}{s/w_1 + 1} \tag{2.1}$$

where $\tau_1 = R_1 C_2$ and $w_1 = 1/\tau_1$. The magnitude of the frequency response is given as

$$|H(jw)| = [1 + (wR_1C_2)^2]^{-1/2} \tag{2.2}$$

and the argument or phase shift is

$$\text{Arg } H(jw) = -\tan^{-1}(wR_1C_2) \qquad (2.3)$$

The frequency response of Figure 2.1 is given in Figure 2.2. As an example $R_1 = 10$ KΩ, $C_2 = 10$ nF, and $w_1 = 10 \times 10^3$ rad sec were chosen to observe the frequency response as a graphical application.

An analog sampled data realization of Figure 2.1 can be obtain by replacing the resistor with one of the switched capacitor equivalent resistances developed in the previous section. But it will be shown that such an equivalence may not hold true when the realizations are used to replace resistors of an RC network.

A. PARALLEL REALIZATION

Figure 2.3(a) shows a switched capacitor RC realization using the parallel SC resistor equivalent of Figure 2.1. To analyze this circuit, the clock sequence has to be identified. Figure 2.3(b) shows the necessary two phase clock sequence. Φ_1 and Φ_2 specify the phase periods during which switches designated as Φ_1 and Φ_2 close and will be denoted as the odd and even phase clocks. The odd phase period can be arbitrarily defined as Φ_1, of the two phase clock. Therefore, the period of time where

$$(n+\iota) \le t/T < (n+\iota+1/2) \qquad \text{odd } (\Phi_1) \text{ phase period}$$
$$(n+\iota+1/2) \le t/T < (n+\iota+1) \qquad \text{even } (\Phi_2) \text{ phase period.}$$

where $\iota = \{...,-2,-1,0,1,...\}$ corresponds to the ιth clock period. The phase periods have been defined to include the left end point only. This convention assures that the nonoverlapping property is preserved. In the analysis of Figure 2.3(a), it will be assumed that $v_1(t)$ is constant during each phase period. Let us consider first the odd phase period where

$$(n-1) \le t/T < (n-1/2)$$

During the operation of the switch Φ_1, it will be assumed that the switch Φ_1 closes immediately after $t = (n-1)T$ and that C_1 is instantaneously charged to $v_1^o[(n-1)T]$. In practice, the time required for v_1 to charge this voltage value should be small compared to T/2. The same situation can also be applied to the Φ_2 switch during its phase period. The only concern is that the switches must be closed long enough to transfer the charge. Otherwise the clock circuits would face very severe timing requirements.

During the odd phase perid Φ_1, Figure 2.3(a) can be redrawn as shown in Figure 2.4(a). From this figure it is seen that

$$v_{c1}(t) = v_1^o[(n-1)T] = v_1^o(n-1) \qquad (2.4)$$

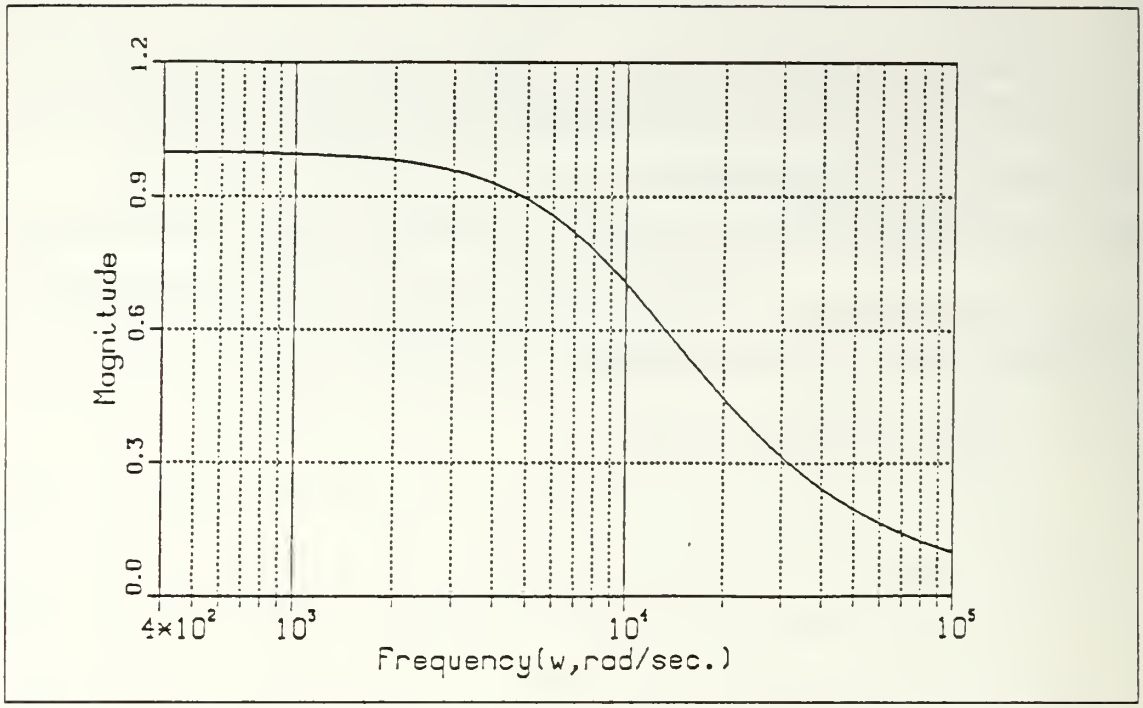

Figure 2.2 (a) The Magnitude Response of the Circuit of Figure 2.1.

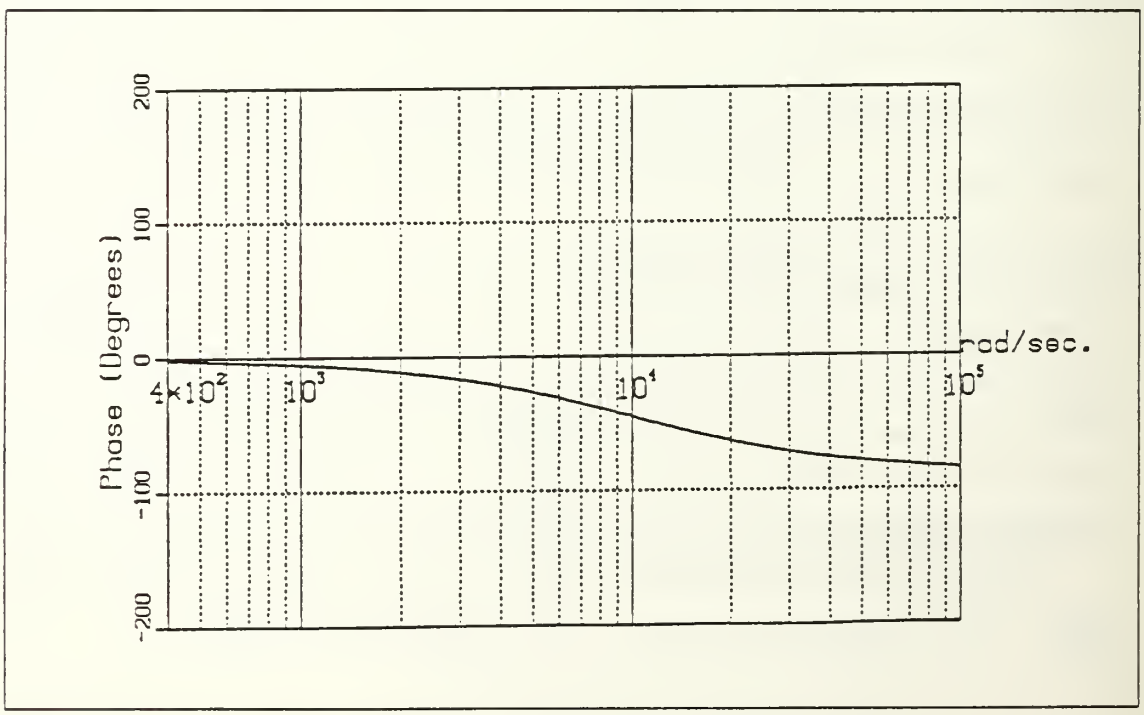

Figure 2.2 (b) The Phase Response of the Circuit of Figure 2.1.

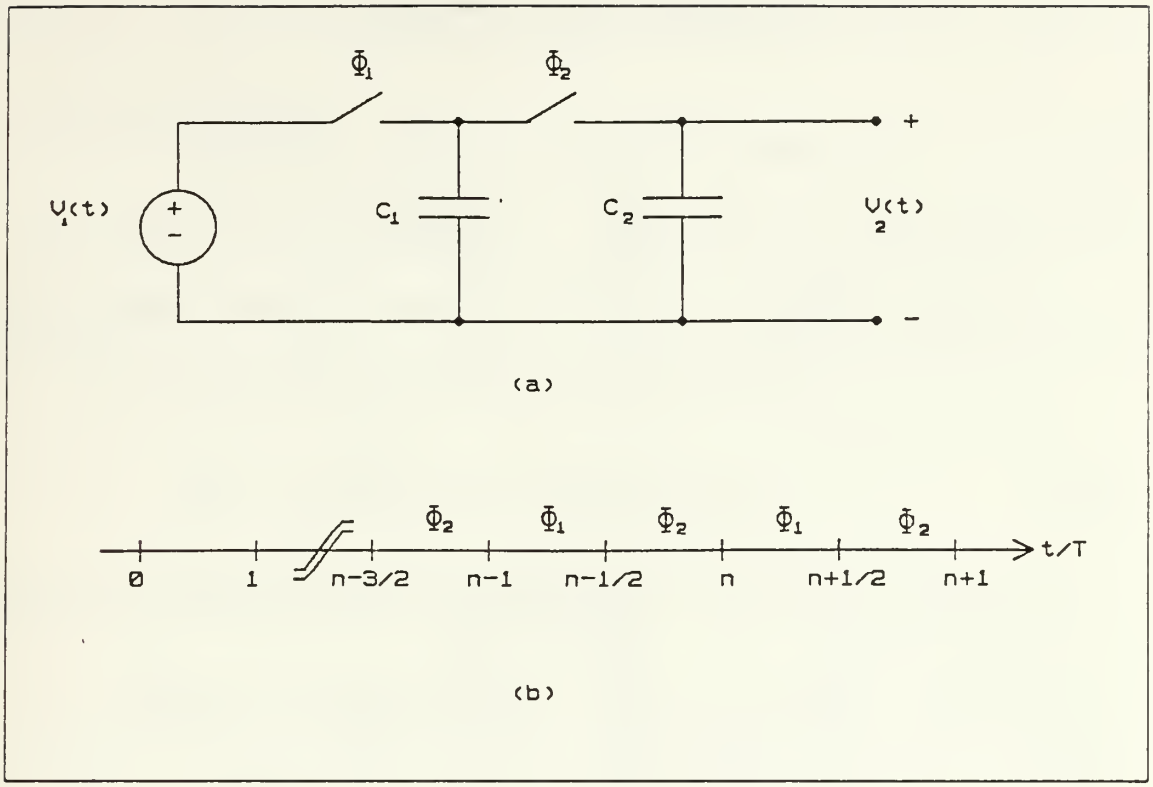

Figure 2.3 Switched Capacitor Realization of Figure 2.1.
(a) Parallel Configuration. (b) Clock Phasing.

$$v_{C2}(t) = v_2^{\circ}[(n-1)T] = v_2^{\circ}(n-1) \tag{2.5}$$

After this point the clock period T in Equation 2.4 and Equation 2.5 will be dropped because it adds no useful information and simplifies the notation.

In the next even phase period $(n-1/2) \leq t/T < n$, the Φ_1 switch is open, and the Φ_2 switch closes. Figure 2.4(b) represents Figure 2.3(a) during this phase period. At the same time C_1 and C_2 are paralleled, resulting in a new value of v_2. Figure 2.4(b) is converted to Figure 2.4(c) with uncharged capacitors and the voltage sources representing the initial voltages on the capacitors. Using superposition techniques, it can be solved for the voltage v_2 to get

$$v_2(t) = \frac{C_1}{C_1+C_2} v_1^{\circ}(n-1) + \frac{C_2}{C_1+C_2} v_2^{\circ}(n-1) \tag{2.6}$$

if $v_2(t)$ is evalutated at $t=(n-1/2)$,

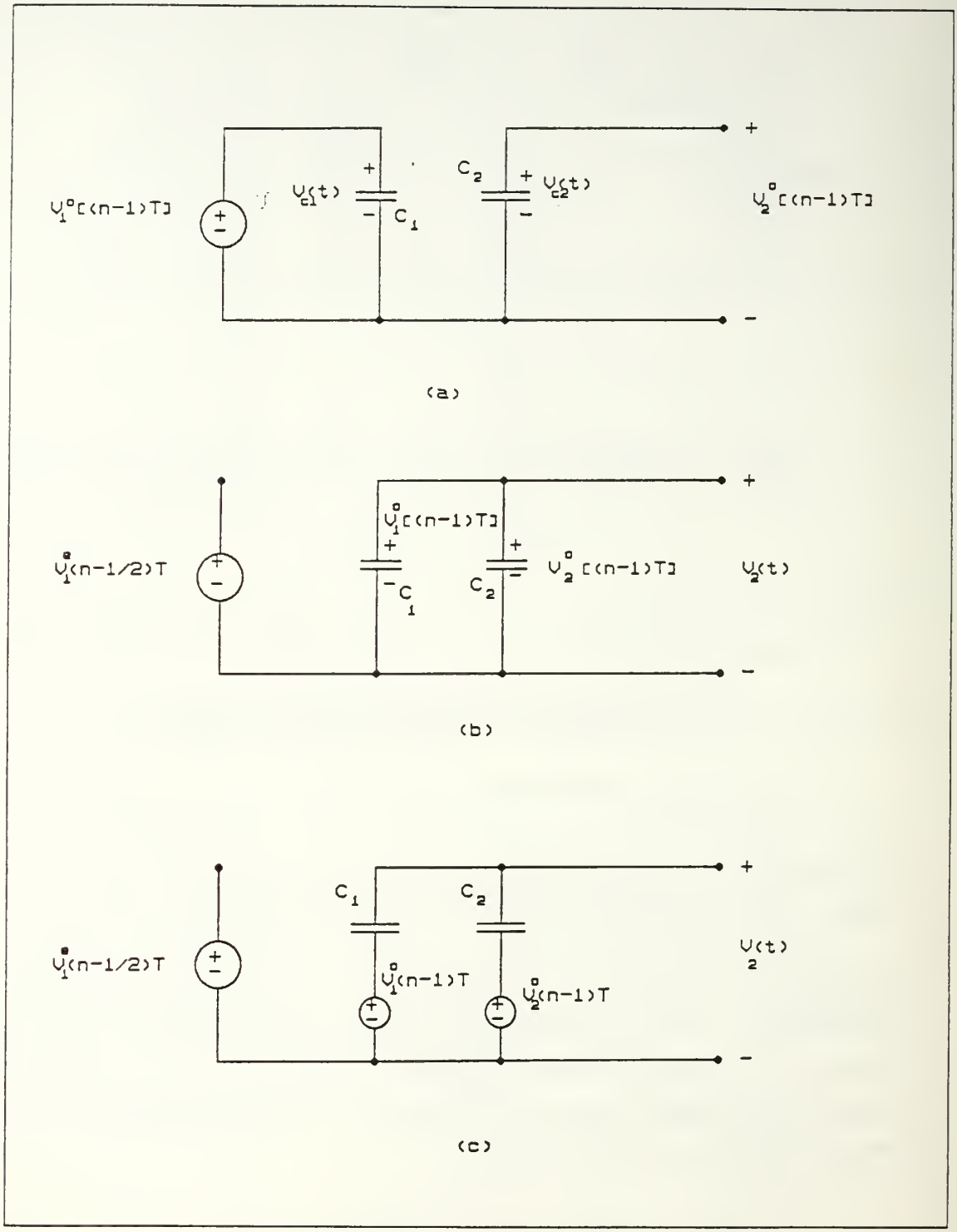

Figure 2.4 Equivalent Circuit of Figure 2.3.
(a) Equivalent Odd Circuit when Φ_1 switch is closed. (b) Equivalent even circuit when Φ_2 switch is closed. (c) Alternative form of (b).

$$v_2^e(n\text{-}1\ 2) = \frac{C_1}{C_1+C_2} v_1^o(n\text{-}1) + \frac{C_2}{C_1+C_2} v_2^o(n\text{-}1) \tag{2.7}$$

At the next phase period,

$$v_2^o(n) = v_2^e(n\text{-}1\ 2) \tag{2.8}$$

using Equation 2.8 and the relationships of Table 1 in Appendix A, Equation 2.7 can be written as

$$V_2^o(z) = \frac{C_1 z^{-1}}{C_1+C_2} V_1^o(z) + \frac{C_2 z^{-1}}{C_1+C_2} V_2^o(z) \tag{2.9}$$

Solving for $V_2^o(z)\ V_1^o(z)$ results in the transfer function $H^{oo}(z)$ for odd-odd case.

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \frac{1}{1+\alpha} \frac{z^{-1}}{1\text{-}\alpha(1+\alpha)^{-1}z^{-1}} \tag{2.10}$$

$$H^{oo}(z) = \frac{1}{(1+\alpha)z\text{-}\alpha} \tag{2.11}$$

where $\alpha = C_2\ C_1$. From Equation 2.8

$$V_2^o(z) = z^{-1\ 2} V_2^e(z) \tag{2.12}$$

$$H^{oo}(z) = \frac{V_2^e(z)}{V_1^o(z)} = \frac{1}{1+\alpha} \frac{z^{-1\ 2}}{1\text{-}\alpha(1+\alpha)^{-1}z^{-1}} \tag{2.13}$$

thus

$$H^{oo}(z) = z^{-1/2} H^{oe}(z) \tag{2.14}$$

since $v_1^o(n) = v_1^e(n)$, the other two possible transfer functions are

$$H^{eo}(z) = \frac{V_2^{o}(z)}{V_1^{e}(z)} = \frac{V_2^{o}(z)}{V_1^{o}(z)} = H^{oo}(z) \tag{2.15}$$

$$H^{ee}(z) = \frac{V_2^{e}(z)}{V_1^{e}(z)} = \frac{V_2^{e}(z)}{V_1^{o}(z)} = H^{oe}(z) \tag{2.16}$$

The method used to determine the transfer function of the analog sampled data realization of the circuit of Figure 2.1 is called conventional network analysis method, [Ref. 2]. There is another approach called charge conservation, [Ref. 4], which is basically an application of Kirchoff's current law, where charge is used instead of current. The method characterizes the charge conservetion condition at a particular node for all time instants of one period, T. The two nodal charge equations can be written for one node, for the odd clock phase

$$q_L^{o}(t') = q_m^{e}(t) + q_c^{o,e}(t), \qquad t' > t \tag{2.17}$$

and for the even clock phase

$$q_L^{e}(t') = q_m^{o}(t) + q_c^{o,e}(t), \qquad t' > t \tag{2.18}$$

where t' is a time reference, $q_L(t')$ is the charge left at one particular node at equilibrium, $q_m(t)$ is the charge at that particular node from the previous phase period called as the memory charge, and $q_c(t)$ is contribution charge injected at that particular node. The superscripts of $q_c^{o,e}(t)$ imply that the contribution charge can be from the even or odd clock phases or both.

Let us analyze the circuit in Figure 2.3(a) using the charge conservation method. The components of Equation 2.18 can be identified as

$$q_L^{e}(n\text{-}1/2) = (C_1 + C_2)v_2^{e}(n\text{-}1/2)$$
$$q_m^{o}(n\text{-}1) = C_2 v_2^{o}(n\text{-}1)$$
$$q_c^{o}(n\text{-}1) = C_1 v_1^{o}(n\text{-}1)$$

and for the next odd phase period

$$q_L^{o}(n) = C_2 v_2^{o}(n)$$
$$q_m^{e}(n\text{-}1/2) = C_2 v_2^{e}(n\text{-}1/2)$$

and since the contribution from the odd phase period is zero, that is,

$$q_c^{o,e}(t) = 0$$

using the above equations and taking the z-transform, the transfer function in Equation 2.10 and Equation 2.13 can be obtained. If Equation 2.18 is written in terms of its components

$$(C_1+C_2)v_2^{e}(n-1/2) = C_2v_2^{o}(n-1)+C_1v_1^{o}(n-1)$$

and the Equation 2.17 in term of its components

$$q_L^{o}(n) = q_m^{e}(n-1/2)$$
$$C_2v_2^{o}(n) = C_2v_2^{e}(n-1/2)$$
$$V_2^{o}(z) = v_2^{e}z^{-1/2}$$
$$(C_1+C_2)V_2^{o}(z) = C_2z^{-1}V_2^{o}(z)+ C_1z^{-1}V_1^{o}(z)$$

$$\frac{V_2^{o}(z)}{V_1^{o}(z)} = \frac{C_1z^{-1}}{(C_1+C_2)-C_2z^{-1}} \tag{2.19}$$

$$H^{oo}(z) = \frac{V_2^{o}(z)}{V_1^{o}(z)} = \frac{z^{-1}}{(1+\alpha)-\alpha z^{-1}} \tag{2.20}$$

Hence, Equation 2.11 was obtained again.

The switched capacitor RC realization of Figure 2.1 has demonstrated a general property of sampled data SC networks. This property is that the z-domain transfer function depends upon which phase period the output is sampled. There are four possible sampled output waveform that can be obtained for a two phase clock scheme.

The next consideration is that whether or not Figure 2.3(a) is an equivalent realization of Figure 2.1. To obtain the specified frequency response in Figure 2.2, how can α be selected? One answer to this question would be to apply the forward transformation of Table 2 in Appendix A to Equation 2.1 to get

$$H(s) \xrightarrow[s=(z-1)/T]{} H(z) = \frac{w_1Tz^{-1}}{1-(1-w_1T)z^{-1}} \tag{2.21}$$

Comparing Equation 2.10 and Equation 2.21 shows that

$$\alpha = \frac{1}{w_1T} - 1 = \frac{1}{2\pi}\frac{w_c}{w_1} - 1 \tag{2.22}$$

This expression would allow α to be designed when $w_c\, w_1$ was specified. To demonstrate the relationship between analog and discrete frequency responses, the frequency response of Equation 2.11 is plotted in Figure 2.5 for $w_c\, w_1 = 10$, which corresponds to $\alpha = 0.5915$, together with the frequency response of Equation 2.1 for $w_1 = 10 \times 10^3$ rad sec in the same graph. To observe the relationship between analog and discrete frequency responses for smaller frequency values, the frequency scale was made in logarithmic scale. Since the sampling frequency, in this case the clock frequency, should be twice the analog signal frequency being sampled, the major concern will be the frequencies that are smaller than the Nyquist rate.The discrete transfer function becomes

$$H(z) = \frac{1}{1.5915z - 0.5915} \tag{2.23}$$

Because of the Nyquist property of the discrete systems, the transfer function of the H(z) is symmetric around $w = 0.5w_c$. Also, for $w < 0.02\ w_c$, the switched capacitor circuit of Figure 2.3(a) is a good approximation of the analog circuit of Figure 2.1. The switched capacitor is a very poor approximation for $w > 0.1\ w_c$. At $w/w_c = 0.5$, the lowest attenuation occurs, and at $w = w_c$ the magnitude is at the starting value. To improve the switched capacitor realization of Figure 2.1, it is necessary to increase w_c or alternatively reduce w_1. To show this property of SC configuration, the frequency response of Equation 2.11 is plotted in Figure 2.6 for $w_c\, w_1 = 50$, which corresponds to $\alpha = 6.9577$, together with the frequency response of Equation 2.1 for $w_1 = 2 \times 10^3$ rad sec, in the same graph. The discrete transfer function becomes

$$H(z) = \frac{1}{7.9577z - 6.9577} \tag{2.24}$$

From the Figure 2.6, much better correlation in the frequency range around w_1 can be observed. Since w_1 was reduced by 5, the discrete transfer function got closer to the continuous transfer function, thus, improving the realization.

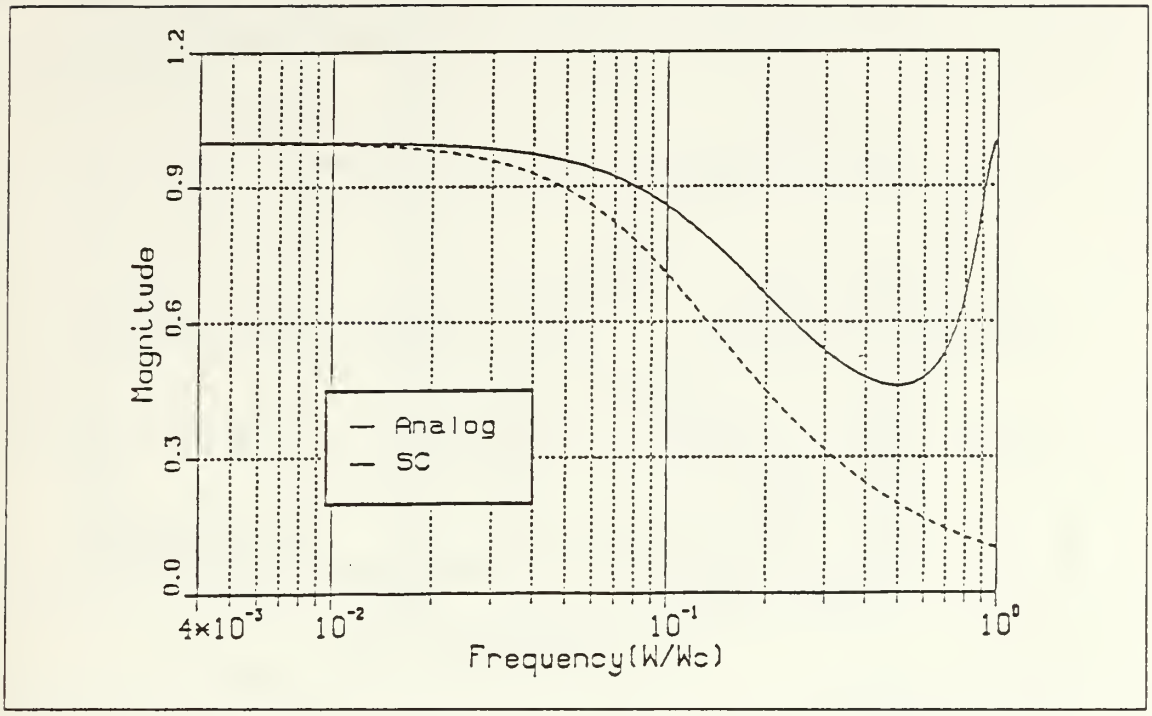

Figure 2.5 (a) Magnitude Response of Equation 2.23.

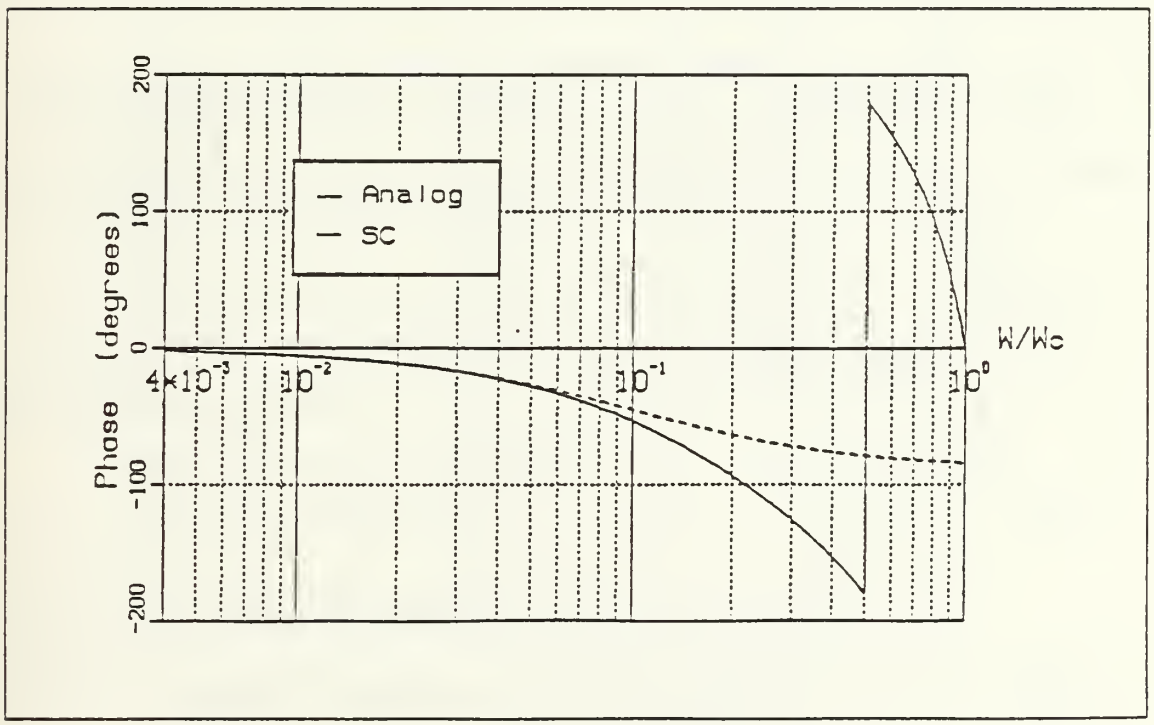

Figure 2.5 (b) Phase Response of Equation 2.23.

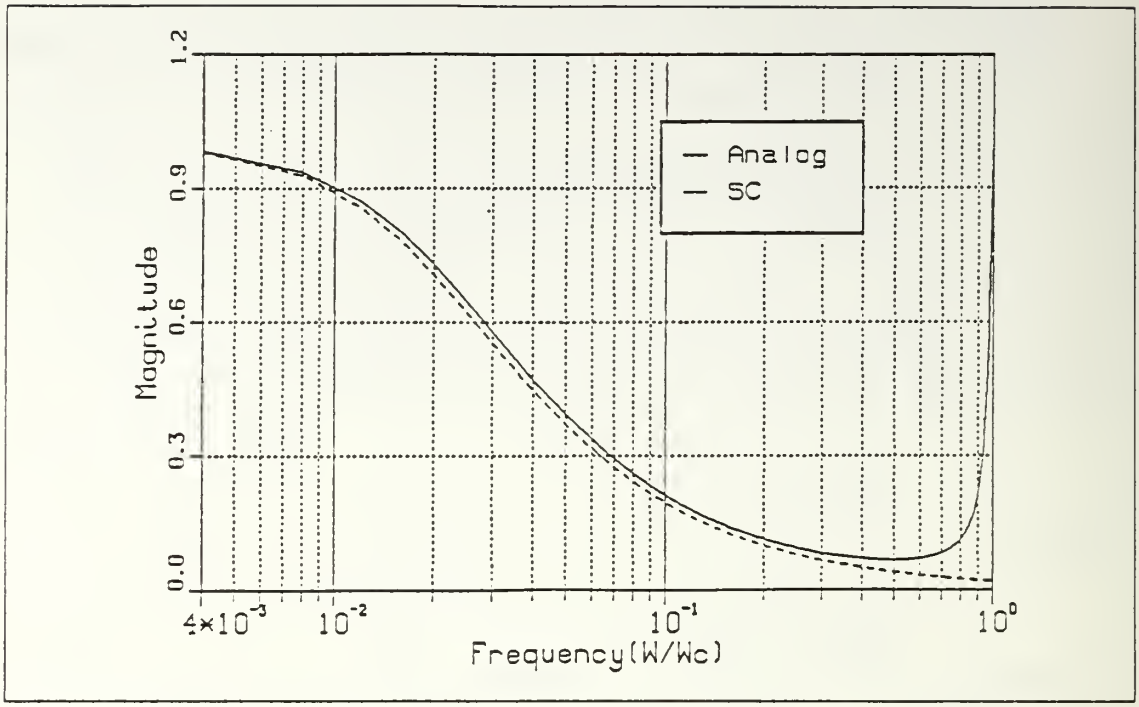

Figure 2.6 (a) Magnitude Response of Equation 2.24.

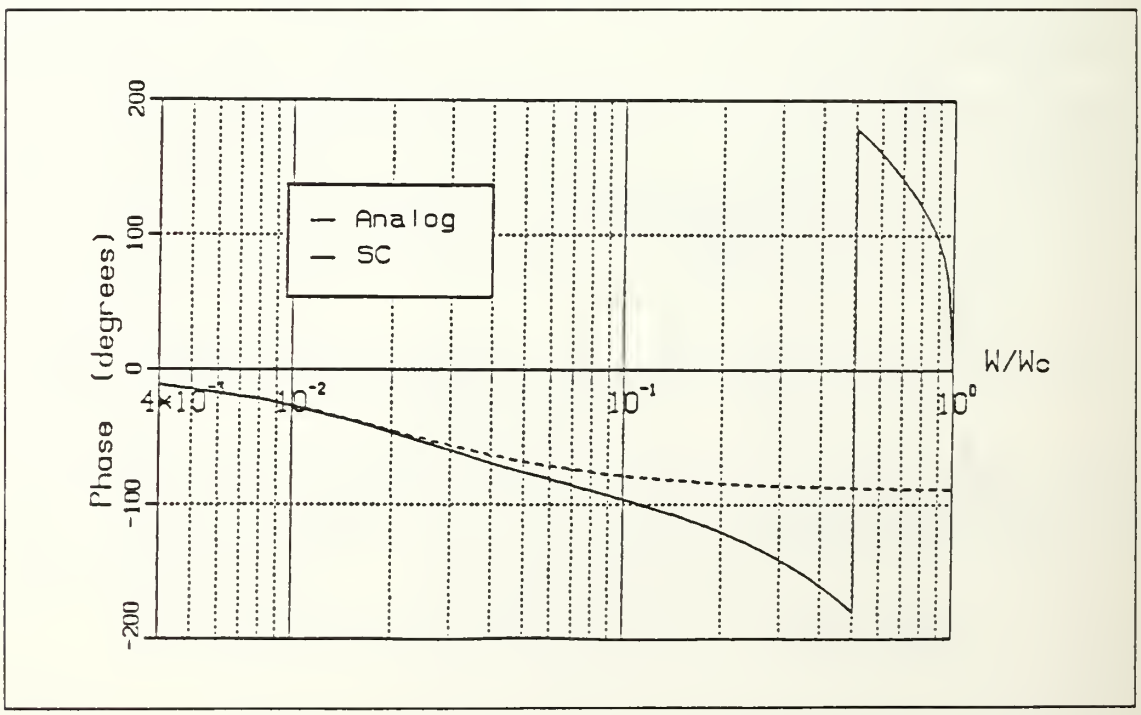

Figure 2.6 (b) Phase Response of Equation 2.24.

B. SERIAL REALIZATION

Another switched capacitor network with a series SC resistor equivalent is shown in Figure 2.7(a).

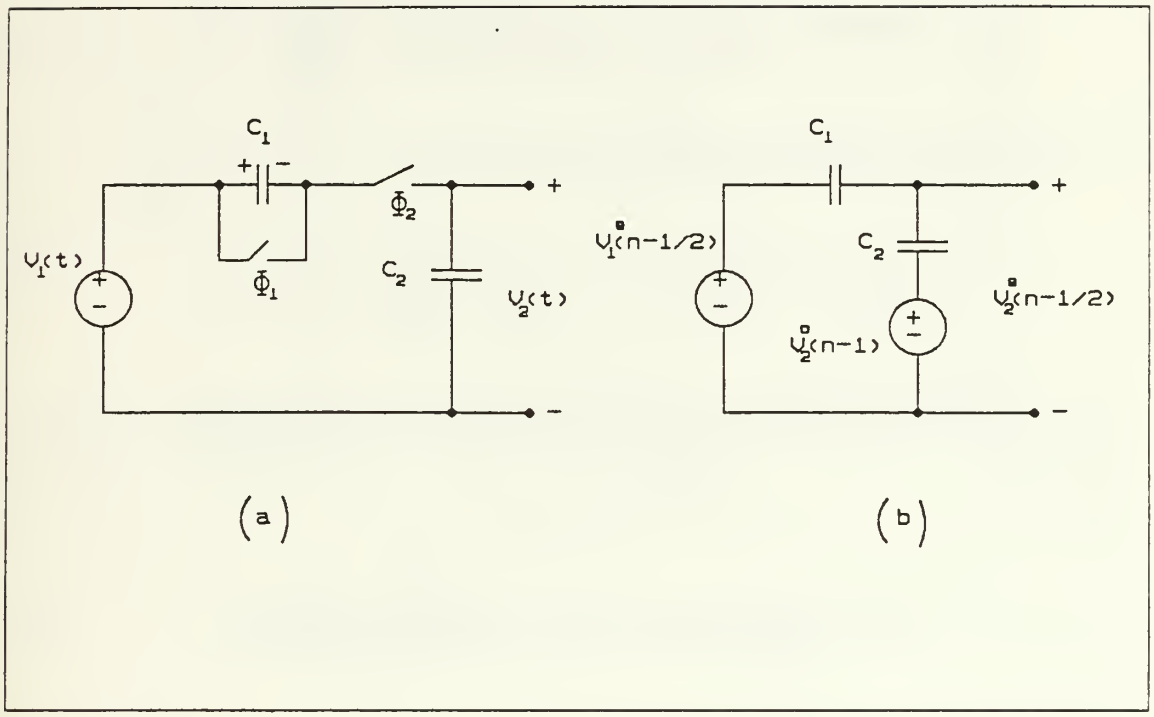

Figure 2.7 Series Switched Capacitor Realization of Figure 2.1.
(a) RC Equivalent Network (b) Equivalent Circuit of (a) for Even Phase Period.

Using charge conservation analysis, for $(n-1/2) \leq t/T < n$, i.e., for the even phase period where Φ_1 is off and Φ_2 is on, we can equate the charges as

$$C_2 v_2^e(n-1/2) = C_2 v_2^o(n-1) + C_1[v_1^e(n-1/2) - v_2^e(n-1/2)] \tag{2.25}$$

and for the odd phase period

$$C_2 v_2^o(n) = C_2 v_2^e(n-1/2) \tag{2.26}$$

By combining Equations 2.25 and 2.26 we obtain

$$C_2 v_2^o(n) = C_2 v_2^o(n-1) + C_1[v_1^e(n-1/2) - v_2^o(n)] \tag{2.27}$$

$$V_2^o(z) = V_2^o(z)z^{-1} + (C_1\ C_2)V_1^e(z)z^{-1\ 2} - (C_1\ C_2)V_2^o(z) \qquad (2.28)$$

and the transfer function

$$H^{eo}(z) = \frac{V_2^o(z)}{V_1^e(z)} = \frac{z^{-1\ 2}}{1-\alpha(1+\alpha)^{-1}z^{-1}} \frac{1}{1+\alpha} \qquad (2.29)$$

From Equations 2.26 and 2.29, it can also be written

$$H^{ee}(z) = \frac{V_2^e(z)}{V_1^e(z)} = \frac{1}{1-\alpha(1+\alpha)^{-1}z^{-1}} \frac{1}{1+\alpha} \qquad (2.30)$$

To obtain the frequency response of Figure 2.7(a), it is necessary to relate α to w_1. Applying the backward transformation of Table 2 in Appendix A to Equation 2.1 results in

$$H(s) \xrightarrow[s=(1-z^{-1})/T]{} H(z) = \frac{w_1T(1+w_1T)^{-1}}{1-(1+w_1T)^{-1}z^{-1}} \qquad (2.31)$$

Comparing Equation 2.30 and Equation 2.31 gives

$$\alpha = \frac{1}{w_1T} = \frac{1}{2\pi} \frac{w_c}{w_1} \qquad (2.32)$$

It can be noted that the series switch possesses a zero at the origin. This zero influences the phase response. The frequency response of Equation 2.29 is given in Figure 2.8 for the case of $(w_1 = 0.1w_c)$ together with the analog frequency response for $w_1 = 10 \times 10^3$ rad sec. Since $\alpha = 1.5915$, the transfer function in Equation 2.29 becomes

$$H(z) = \frac{z^{1\ 2}}{2.5915z-1.5915} \qquad (2.33)$$

The frequency response of Equation 2.29 for the case of $(w_1 = 0.02w_c)$ is also given in Figure 2.9 together with the analog frequency response for $w_1 = 2 \times 10^3$ rad sec, $\alpha = 7.9577$, and the transfer function is

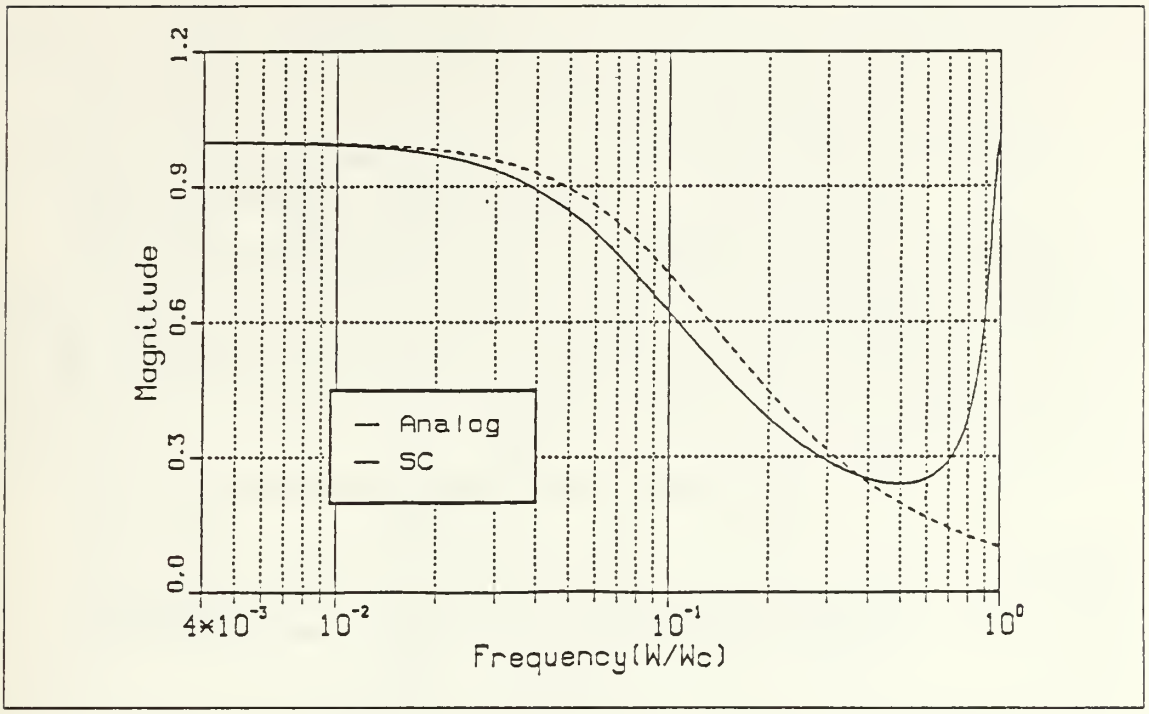

Figure 2.8 (a) Magnitude Response of Equation 2.33.

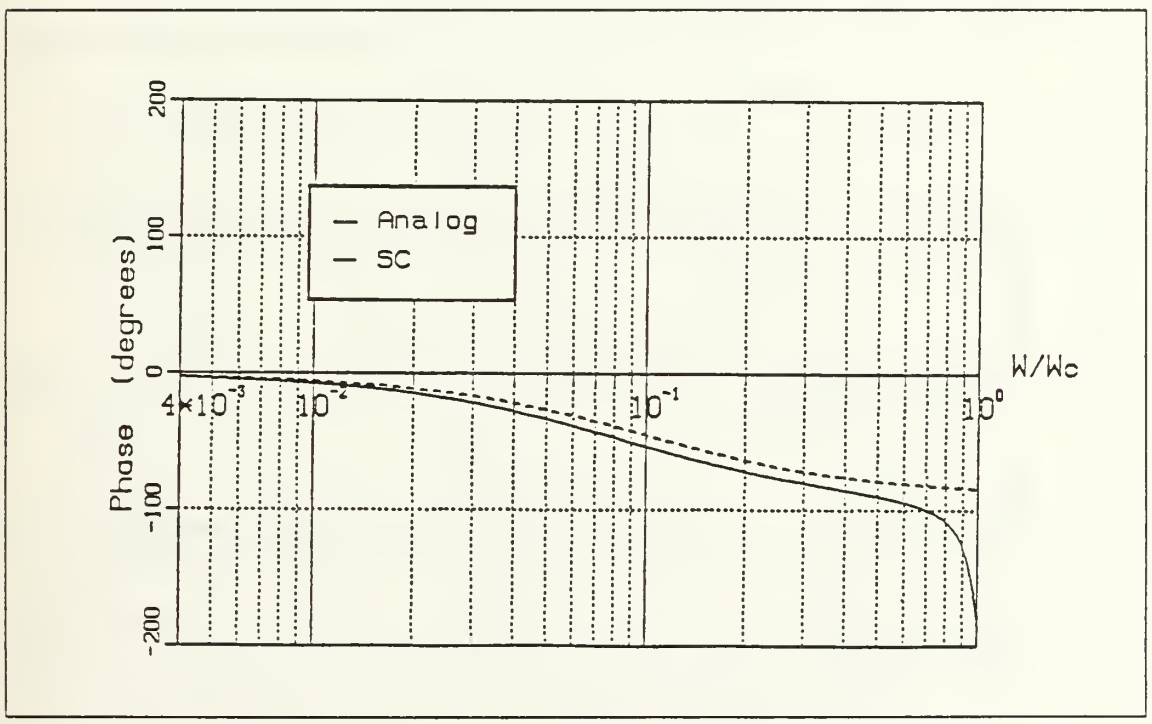

Figure 2.8 (b) Phase Response of Equation 2.33.

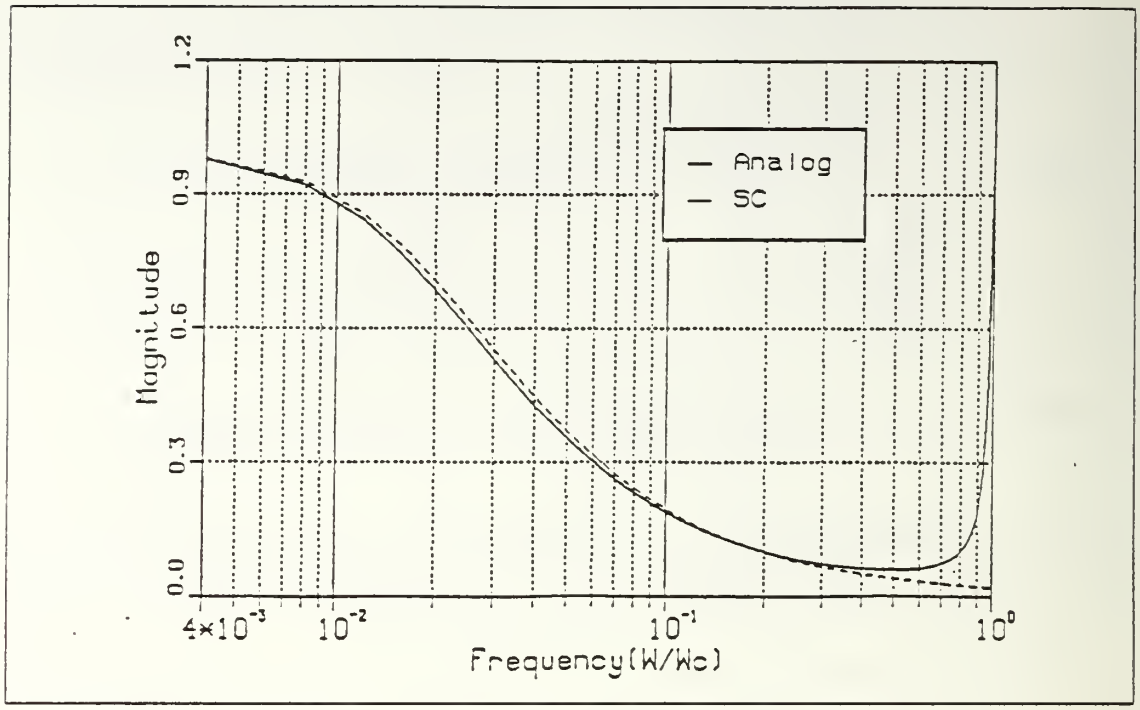

Figure 2.9 (a) Magnitude Response of Equation 2.34.

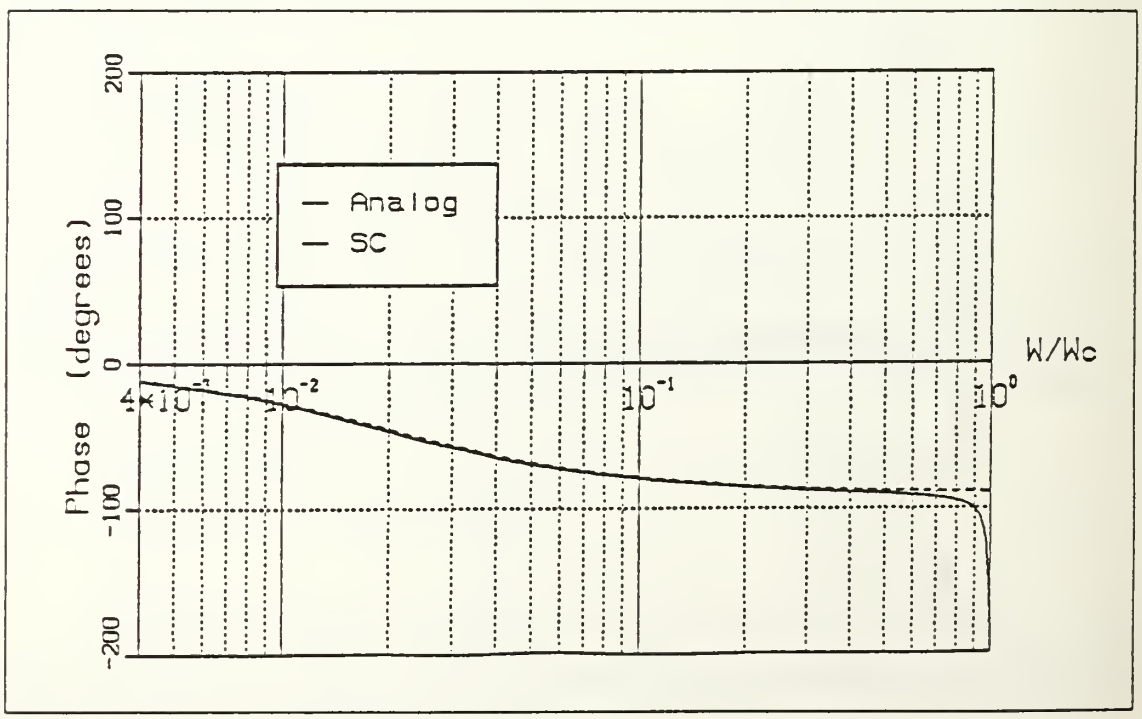

Figure 2.9 (b) Phase Response of Equation 2.34.

$$H(z) = \frac{z^{1/2}}{8.9577z-7.9577} \tag{2.34}$$

it can be seen again that the sampling rate has a strong influence on the results.

C. PARALLEL-SERIAL REALIZATION

Another SC resistor equivalent used to replace the resistor R, in Figure 2.1 is shown in Figure 2.10(a). This implementation uses the series-parallel SC resistor. The equivalent representations of Figure 2.10(a) for the odd and even phase clocks are shown in Figure 2.10(b) and (c). The even phase period Φ_2 occurs between (n-1/2)T and nT.

The charge conservation equation for Φ_2 is given by

$$(C_1+C_2)v_2^e(n-1/2) = C_2v_2^o(n-1)+C_1v_1^o(n-1) + C_1[v_1^e(n-1/2)-v_2^e(n-1/2)] \tag{2.35}$$

Considering the next odd phase clock, it can be observed that

$$v_2^e(n-1/2) = v_2^o(n) \tag{2.36}$$

and it is also assumed that

$$v_1^e(n-1/2) = v_1^o(n) \tag{2.37}$$

Using the relationship of the table of Appendix A and $C_1 = C/2$, $\alpha_1 = C_2/C$ results

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \frac{1}{2(1+\alpha_1)} \frac{1+z^{-1}}{1-\alpha_1(1+\alpha_1)^{-1}z^{-1}} \tag{2.38}$$

It can be seen that there is a zero at z=-1. This zero will result in a notch or zero magnitude at half the sampling frequency. To plot the frequency response and compare it with the analog response of Figure 2.1, it is necessary to develop a relationship between α_1 and w_1. For this purpose, the bilinear transformation of Table 2 in Appendix A is applied to H(s) given by Equation 2.1. The result will be equated to Equation 2.38.

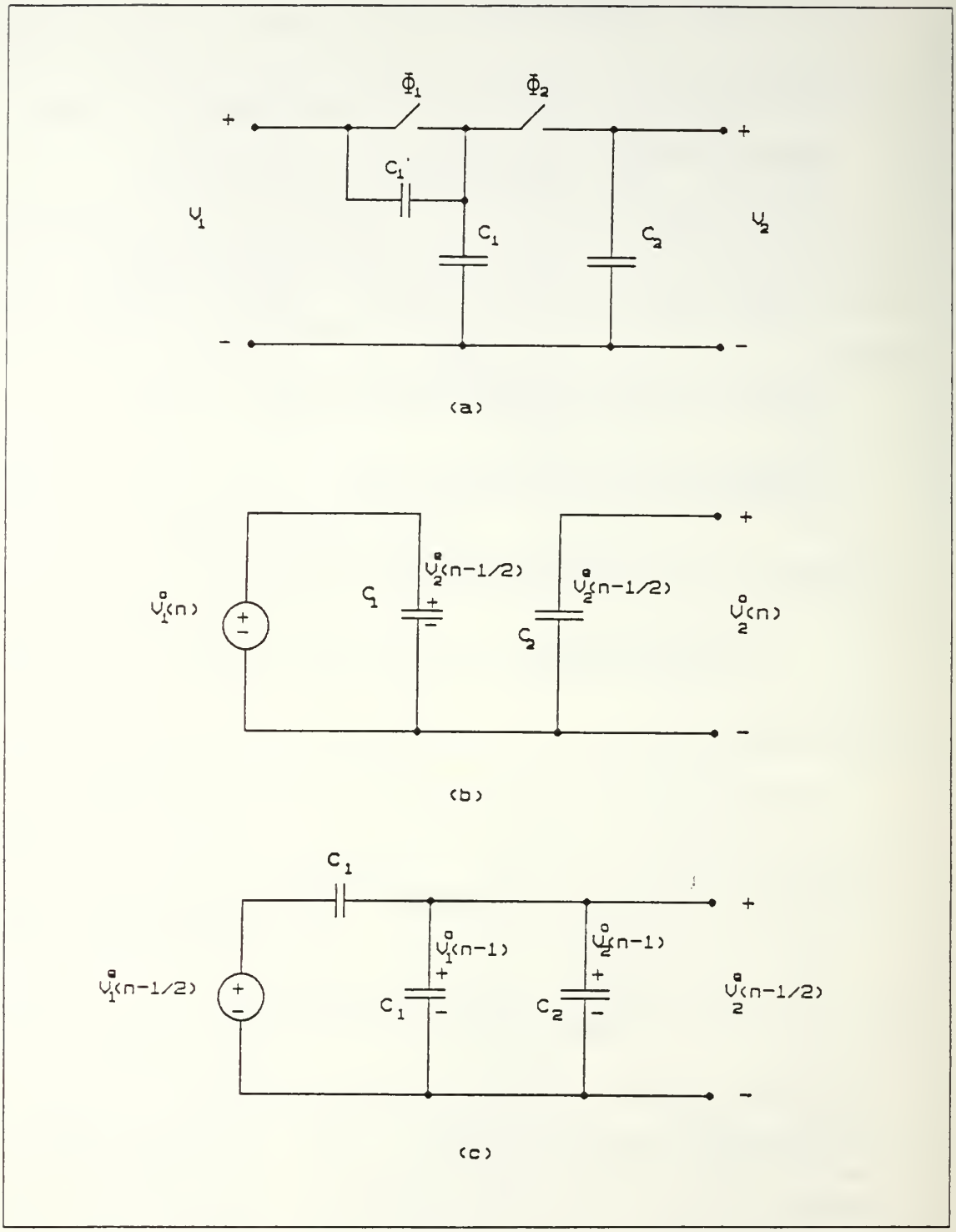

Figure 2.10 Parallel-Series SC Realization of Figure 2.1.
(a) Equivalent SC Circuit. (b) Equivalent Representations of (a) when Φ_1 is closed and (c) when Φ_2 is closed.

$$H(s) = \xrightarrow[s=\frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)]{} H(z) = \frac{1+z^{-1}}{1-z^{-1}\dfrac{1-\dfrac{Tw_1}{2}}{1+\dfrac{Tw_1}{2}}} \frac{Tw_1}{1+\dfrac{Tw_1}{2}} \quad (2.39)$$

In this passive RC case, the series-parallel SC resistor equivalent corresponds exactly to the bilinear mapping if

$$2\alpha_1 = \frac{2}{w_1 T} - 1 \quad (2.40)$$

The frequency response of Equation 2.38 is given in Figure 2.11 for the case of $(w_1 = 0.1w_c)$ together with the analog frequency response for $w_1 = 10 \times 10^3$ rad sec. since $\alpha_1 = 1.0915$, the transfer function in Equation 2.38 becomes

$$H(z) = \frac{1}{2} \frac{1+z^{-1}}{(1+\alpha_1)-\alpha_1 z^{-1}} \quad (2.41)$$

$$H(z) = \frac{0.5z+0.5}{2.0915z-1.0915} \quad (2.42)$$

The frequency response of Equation 2.38 for the case of $(w_1 = 0.02w_c)$ is also given in Figure 2.12 together with the analog frequency response for $w_1 = 2 \times 10^3$ rad sec., $\alpha_1 = 7.4577$, and the transfer function in Equation 2.38 becomes

$$H(z) = \frac{0.5z+0.5}{8.4577z-7.4577} \quad (2.43)$$

D. BILINEAR REALIZATION

The last SC realization of Figure 2.1 to be considered is shown in Figure 2.13(a) and uses the bilinear SC resistor simulation. Figure 2.13(b) and (c) show an equivalent circuit for Figure 2.13(a) during the Φ_2 and Φ_1 phase periods, respectively

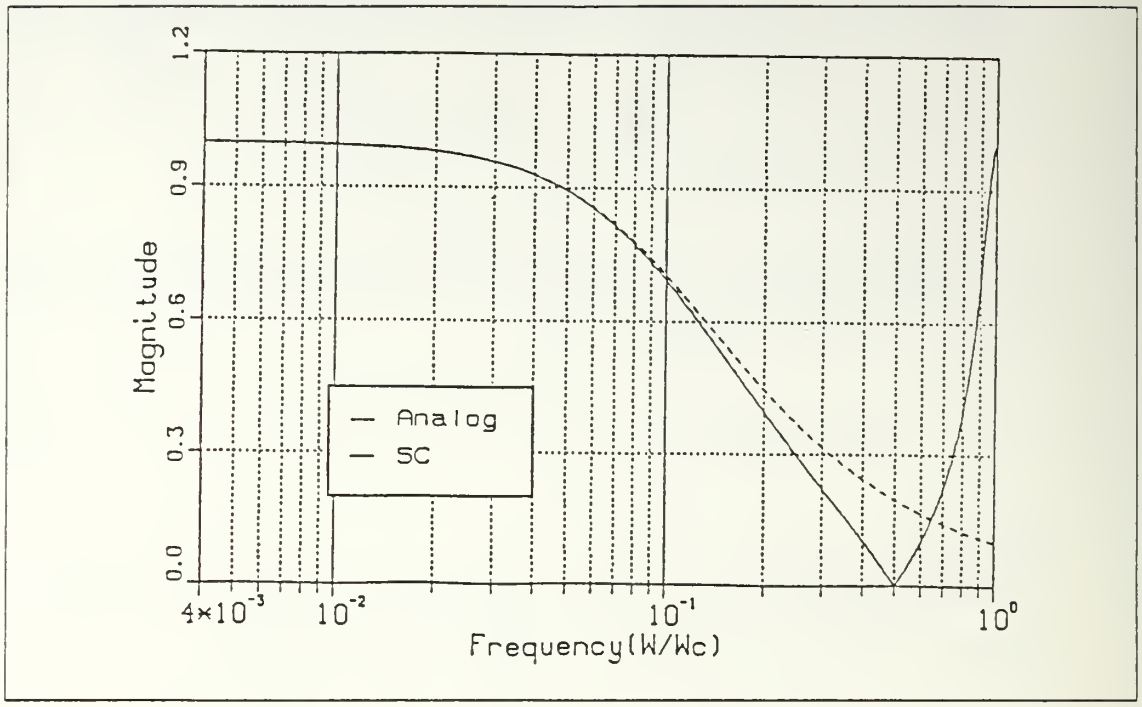

Figure 2.11 (a) Magnitude Response of Equation 2.42.

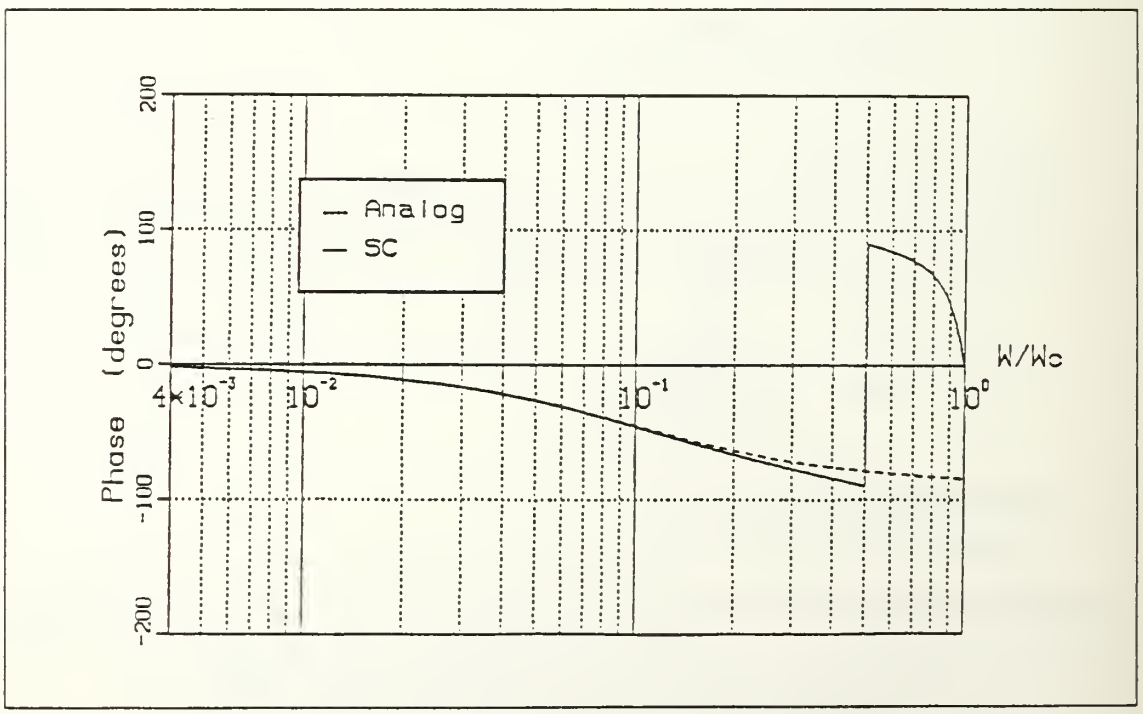

Figure 2.11 (b) Phase Response of Equation 2.42.

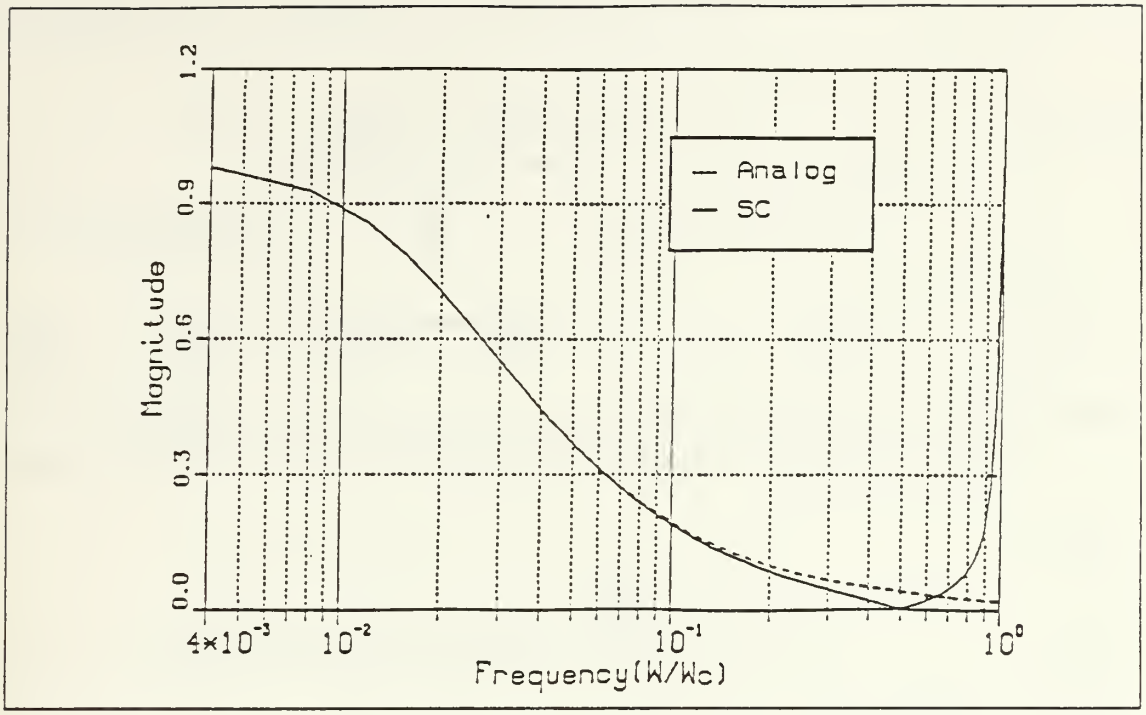

Figure 2.12 (a) Magnitude Response of Equation 2.43.

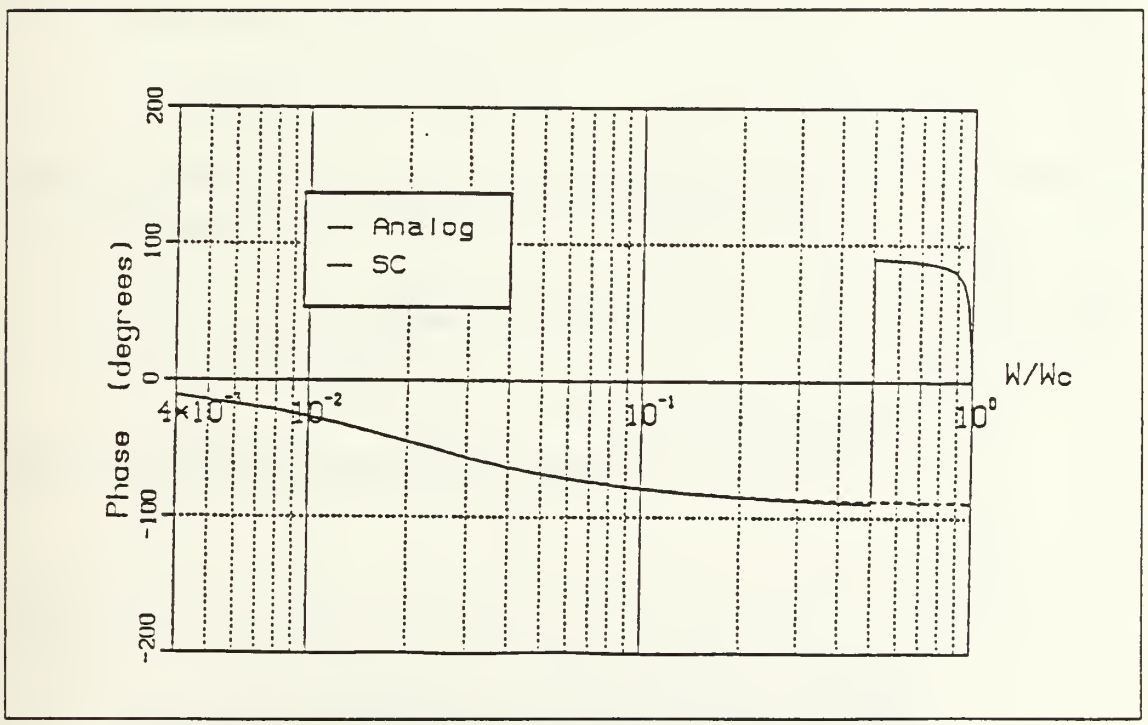

Figure 2.12 (b) Phase Response of Equation 2.43.

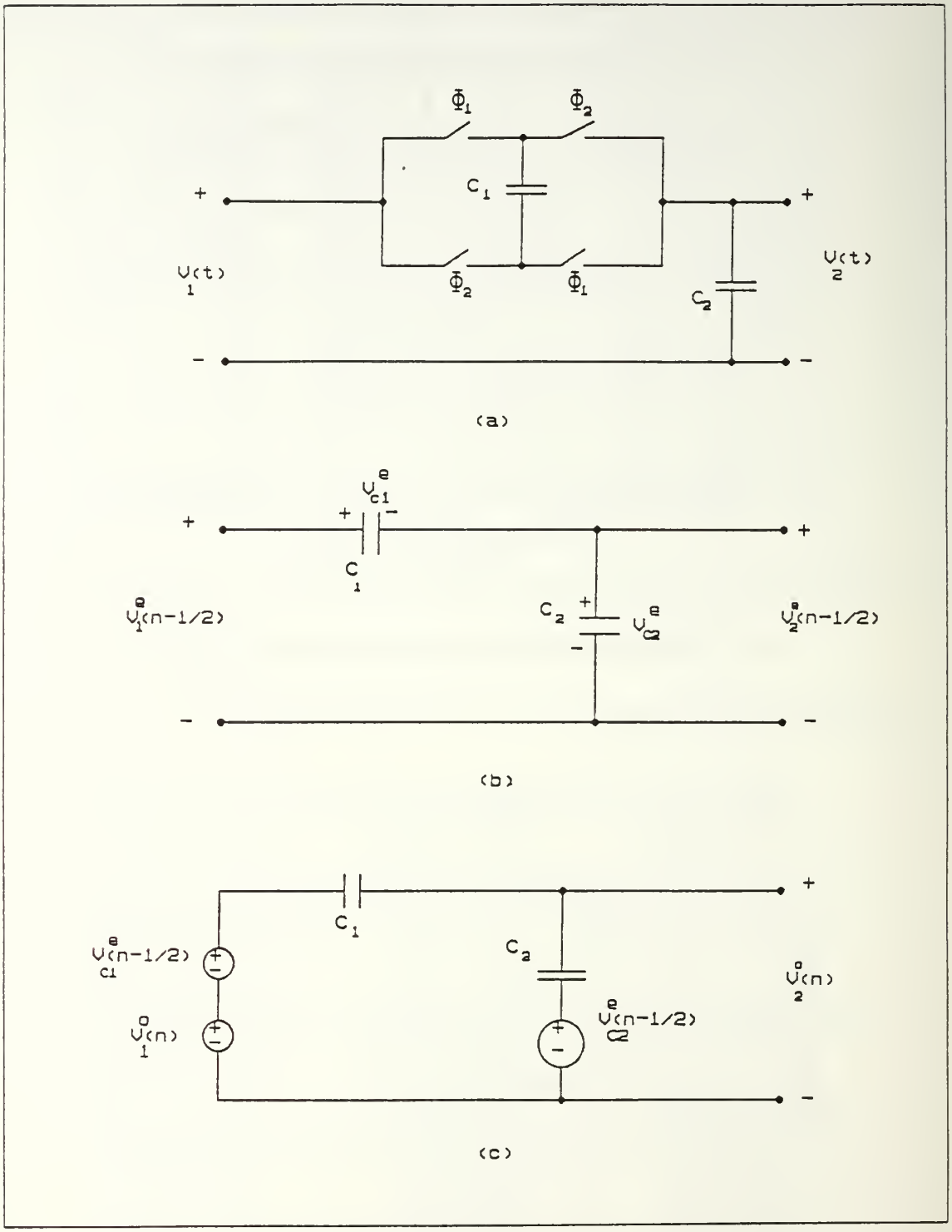

Figure 2.13 Bilinear SC Resistor Simulation of Figure 2.1 (a) Equivalent SC Circuit (b) An Equivalent Circuit for (a) during the Φ_2 Phase Period (c) During the Φ_1 Phase Period.

If the even phase period Φ_2 occurs between (n-1/2)T and nT, C_1 is charged to the voltage

$$v_{c1}^{e}(n-1/2) = v_1^{e}(n-1/2)-v_2^{e}(n-1/2) \tag{2.44}$$

and C_2 is charged to

$$v_{c2}^{e}(n-1/2) = v_2^{e}(n-1/2) \tag{2.45}$$

At the beginning of the next odd phase Φ_1, $n \leq t/T < (n+1/2)$, using the charge conservation approach, the component of Equation 2.17 can be identified as

$$q_L^{o}(n) = C_2 v_2^{o}(n) \tag{2.46}$$

$$q_m^{e}(n-1/2) = C_2 v_2^{e}(n-1/2) \tag{2.47}$$

$$q_c^{o,e} = C_1 v_{c1}^{e}(n-1/2) + C_1 v_{c1}^{o}(n) \tag{2.48}$$

where

$$v_{c1}^{o}(n) = v_1^{o}(n)-v_2^{o}(n) \tag{2.49}$$

Combining Equations 2.46, 2.47, 2.48, 2.49, and using the z-transform, Equation 2.17 can be written as

$$(C_1+C_2)V_2^{o}(z) = z^{-1/2}(C_2-C_1)V_2^{e}(z) + C_1[V_1^{e}(z)z^{-1/2} + V_1^{o}(z)] \tag{2.50}$$

Similarly, the following equation can be obtained

$$(C_1+C_2)V_2^{e}(z) = z^{-1/2}(C_2-C_1)V_2^{o}(z) + C_1[V_1^{o}(z)z^{-1/2} + V_1^{e}(z)] \tag{2.51}$$

during the even phase period. By summing Equation 2.50 and Equation 2.51 the transfer function can be obtained as

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{V_2^e(z)\, V_2^o(z)}{V_1^e(z) + V_1^o(z)} = \frac{1 + z^{-1/2}}{(1+\alpha) + (1-\alpha) z^{-1/2}} \qquad (2.52)$$

where $\alpha = C_2 / C_1$.

In the bilinear SC resistor simulation, a complete clock period is really $T_c/2$, rather than T because the input signal is sampled twice in a single clock period. If a new period is defined as

$$T' = T_c / 2$$

then Equation 2.52 can be rewritten

$$H(z) = \frac{z' + 1}{(1+\alpha) z' + (1-\alpha)} = \frac{1}{1+\alpha} \frac{1 + z'^{-1}}{1 - ((\alpha-1)/(\alpha+1)) z'^{-1}} \qquad (2.53)$$

Again, it is necessary to develop a relationship between α and w_1 to plot the frequency response and compare it with the analog response of Figure 2.1. If the bilinear transformation is applied to H(s) in Equation 2.1, the transfer function in the z domain is obtained, using Equation 2.39. By equating it to Equation 2.53 we obtain

$$\alpha = \frac{4}{w_1 T_c} = \frac{2}{\pi} \frac{w_c}{w_1} \qquad (2.54)$$

The frequency response of Equation 2.53 is given in Figure 2.14 for the case of $(w_1 = 0.1\, w_c)$. Since $\alpha = 6.3662$ the transfer function becomes

$$H(z) = \frac{z' + 1}{7.3662 z' - 5.3662} \qquad (2.55)$$

The frequency response of Equation 2.53 for the case of $(w_1 = 0.02 w_c)$ is also given in Figure 2.15. $\alpha = 31.831$, and the transfer function becomes

$$H(z) = \frac{z' + 1}{32.831 z' - 30.831} \qquad (2.56)$$

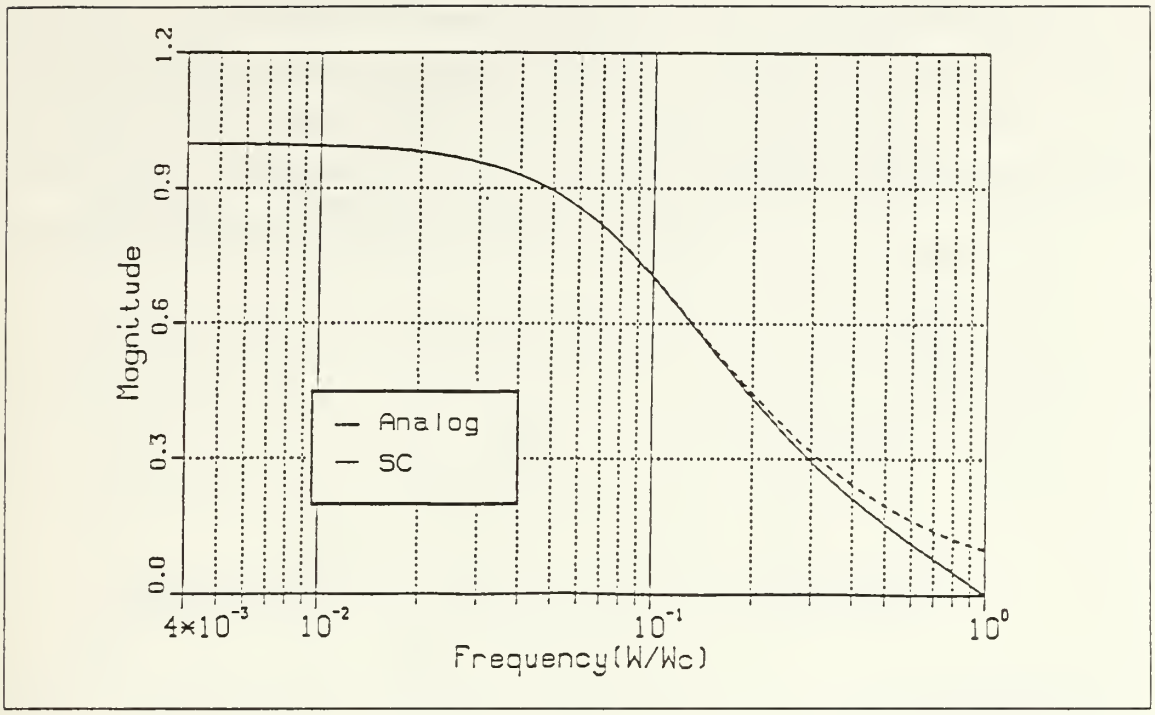

Figure 2.14 (a) Magnitude Response of Equation 2.55.

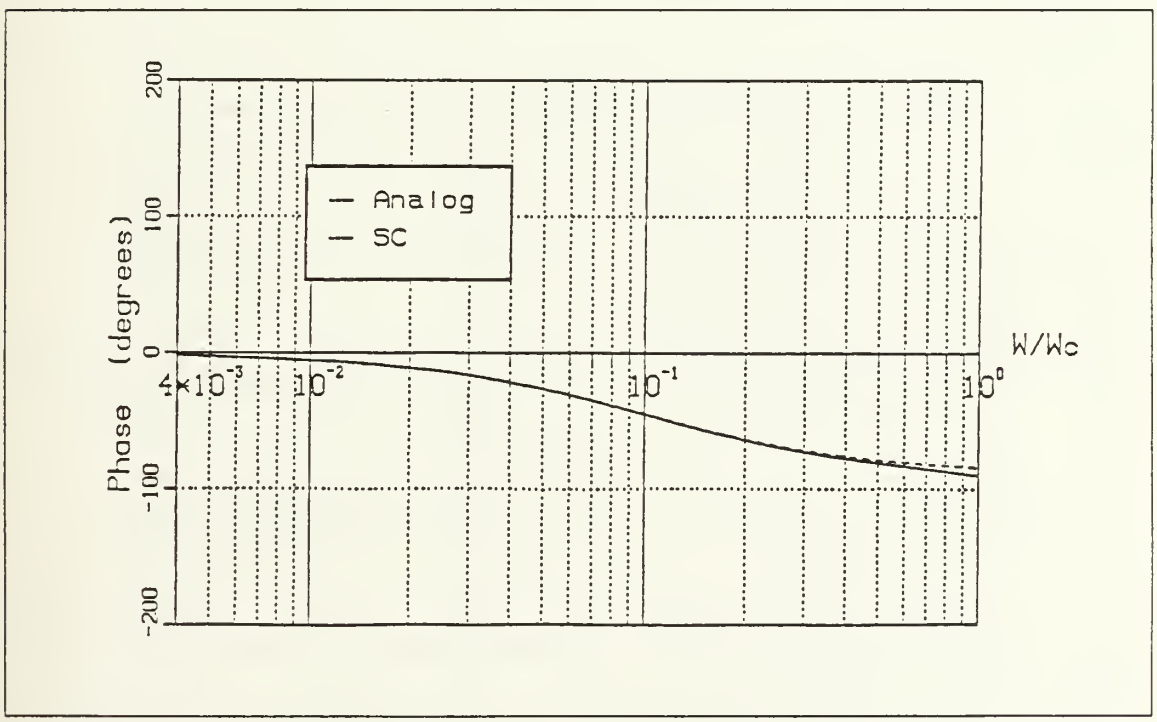

Figure 2.14 (b) Phase Response of Equation 2.55.

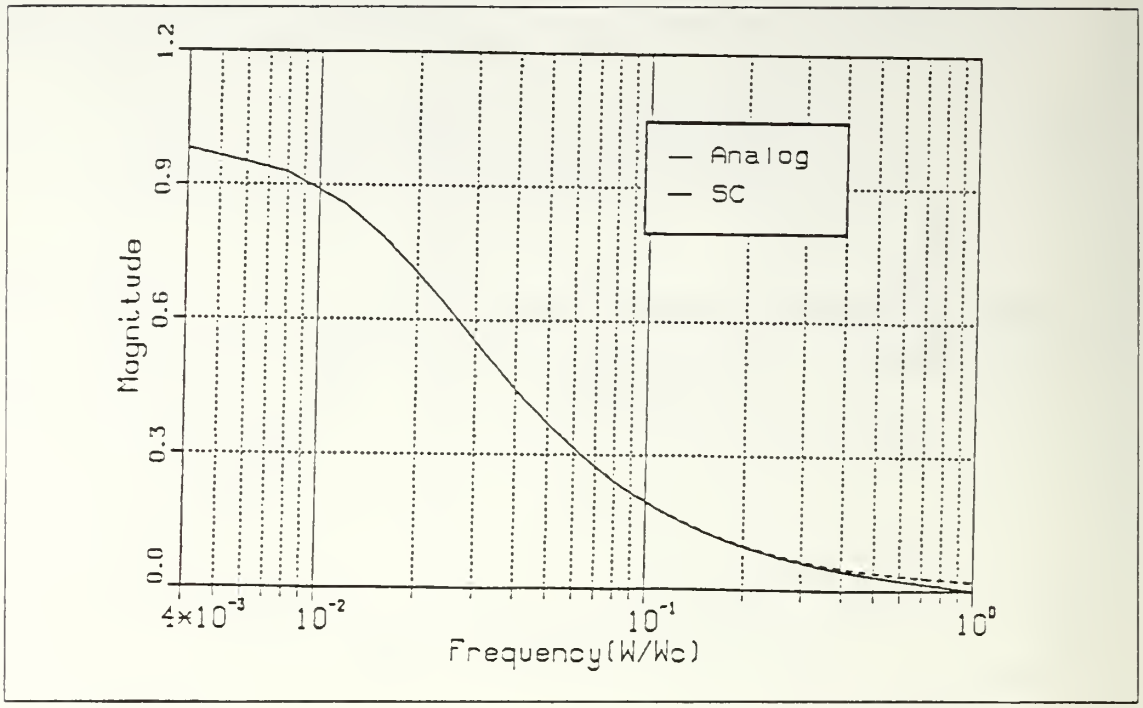

Figure 2.15 (a) Magnitude Response of Equation 2.56.

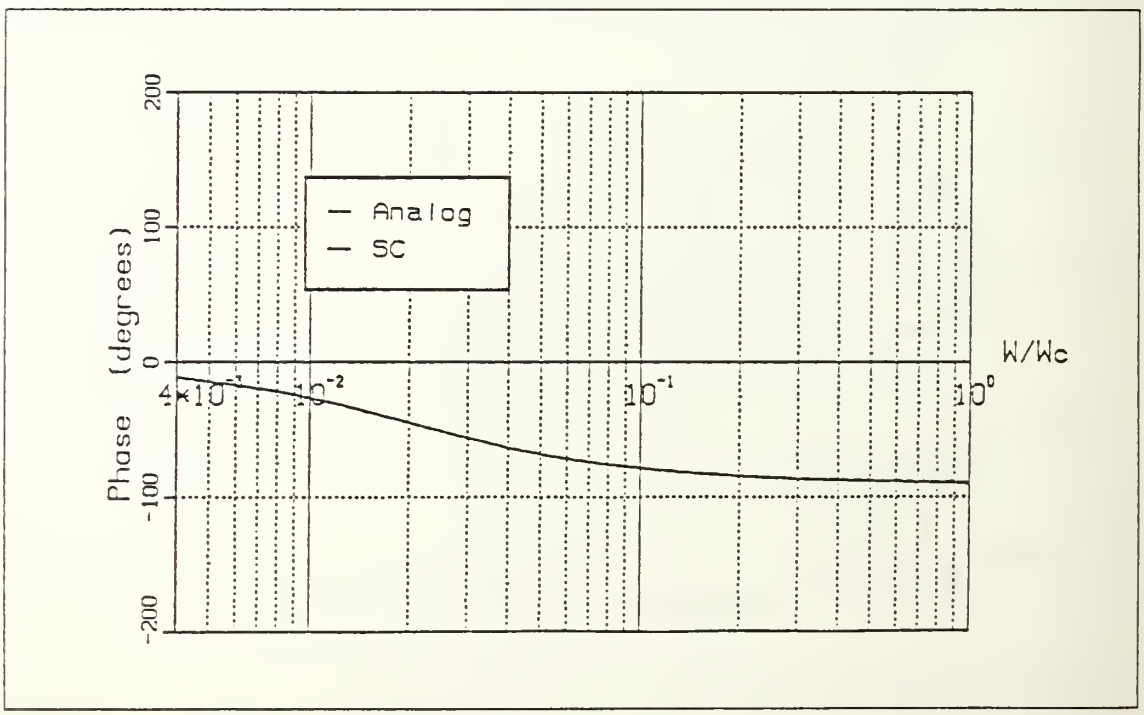

Figure 2.15 (b) Phase Response of Equation 2.56.

In this chapter the use of the SC resistor simulations of Chapter I have been examined by implementing the passive low-pass, first order network of Figure 2.1. This section also illustrated the importance of having the sampling frequency rather high. In Chapter IV a second order switched-capacitor phase-locked loop will be implemented by using the bilinear SC realization since the best SC realization obtained from this chapter is the bilinear SC resistor realization.

III. PHASE-LOCKED LOOP (PLL)

A. LOOP COMPONENTS

The essential elements of a phase-locked loop are the voltage controlled oscillator (VCO), the phase detector, the loop filter and the amplifier.

1. Voltage Controlled-Oscillator (VCO)

In the VCO, an oscillator whose frequency is controlled by a voltage, the amount of change in frequency is directly proportional to the level of the input voltage.

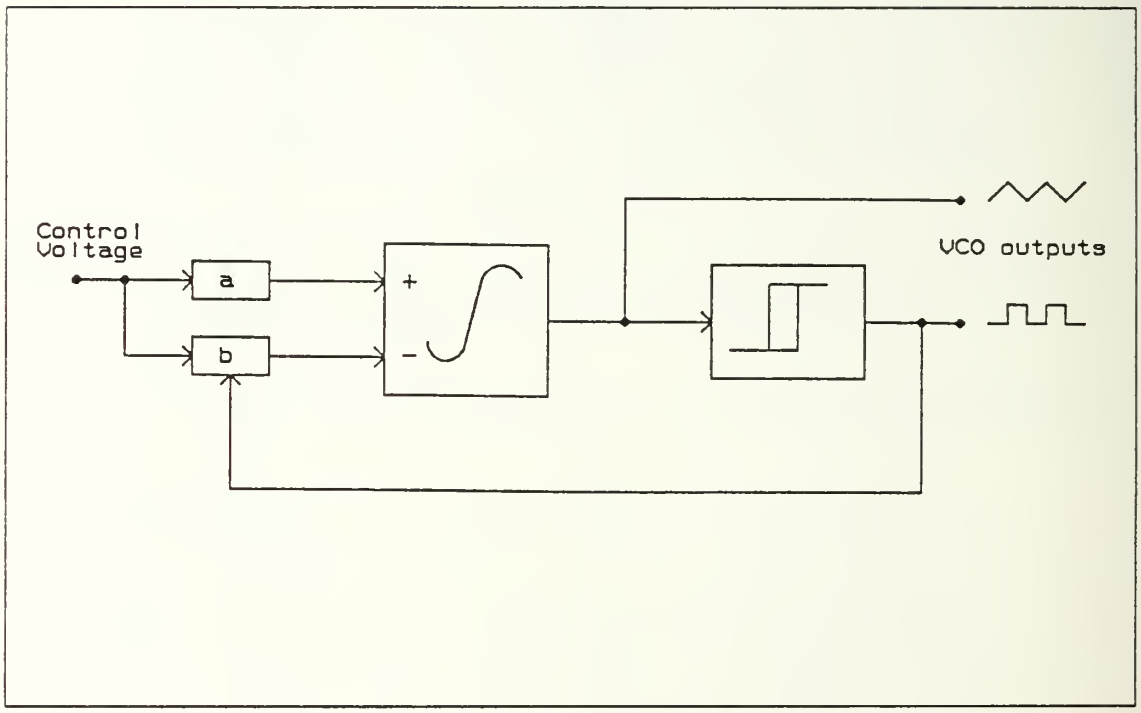

Figure 3.1 Voltage Controlled Oscillator.

As seen in Figure 3.1, the VCO consists of two main elements, one of them is an integrator, the other one is a comparator. As both inputs of the integrator are constant voltages, its output is a ramp whose slope is determined by which terminal, (+) or (-), has the more positive input voltage. The ramp is negative going if the voltage at the (-) terminal is more positive than the voltage at the (+) terminal and vice-versa. By continuously alternating the voltage at the (-) terminal above and below

that of the (+) terminal, a triangular wave is generated at the integrator output. The comparator output is a constant positive or negative voltage, determined by which of the (+) or (-) terminals has the larger voltage. The output is negative whenever the (-) terminal voltage is more positive than the (+) terminal voltage.

Before implementing a SC PLL, an analog PLL was implemented as prototype. The VCO used in the PLL is shown in the Figure 3.2, [Ref. 5], and operates as follows assuming the output of the comparator is initially HIGH.

1. The high level output, v_o, causes the analog switch connected to it to be ON.
2. This causes the voltage on the integrator (-) terminal, v_1, to be equal to $V_c/3$ if we ignore the resistance of the switch. This makes the coefficient, b, in Figure 3.1

$$b = \frac{R/2}{R+R/2} = \frac{1}{3}$$

$$a = \frac{R_1}{2R_1} = \frac{1}{2} \qquad \text{(always)}$$

3. Since $a > b$, the positive input causes the output of the integrator to be a positive going ramp at output v_2, it is also shown in Figure 3.3.
4. At this point the voltage, v_3, at the (+) terminal of comparator is given.

$$v_{31} = \frac{V_{DD}}{R_a+R_b+R_c}\left[\frac{R_b+R_c}{2}+R_a\right] \tag{3.1}$$

When the integrator output exceeds v_3, the comparator output goes low, turning the switch OFF.

5. b is now equal to 1 and $a < b$. This generates a negative going ramp at the output of the integrator. At this point the voltage v_3 is given

$$v_{30} = \frac{R_b}{R_a+R_b}\frac{V_{DD}}{2} \tag{3.2}$$

6. When the output of the integrator goes below v_3, the comparator output, v_0, goes HIGH and the cyle repeats. Using positive feedback on the comparator

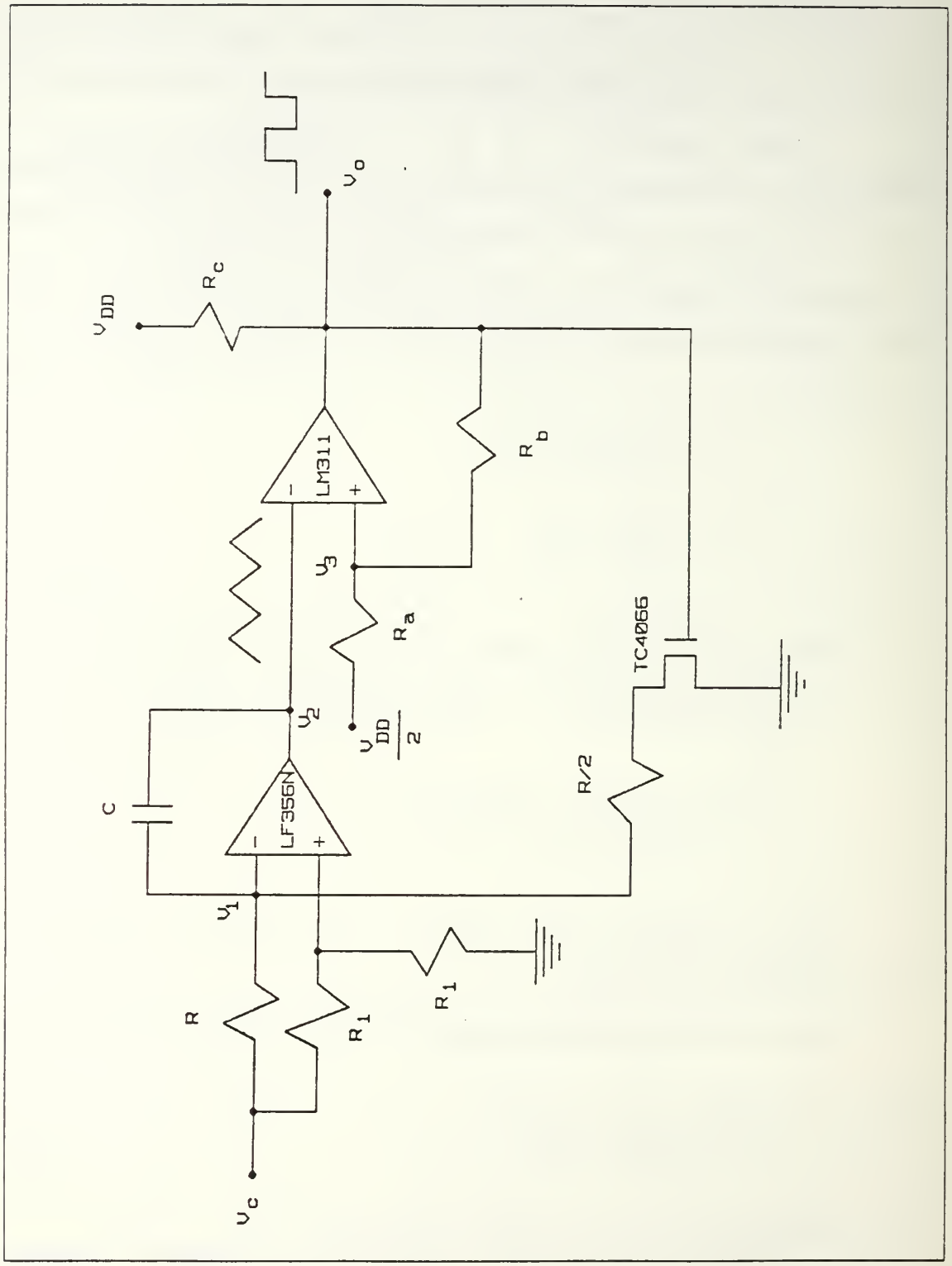

Figure 3.2 Prototype Voltage Controlled Oscillator.

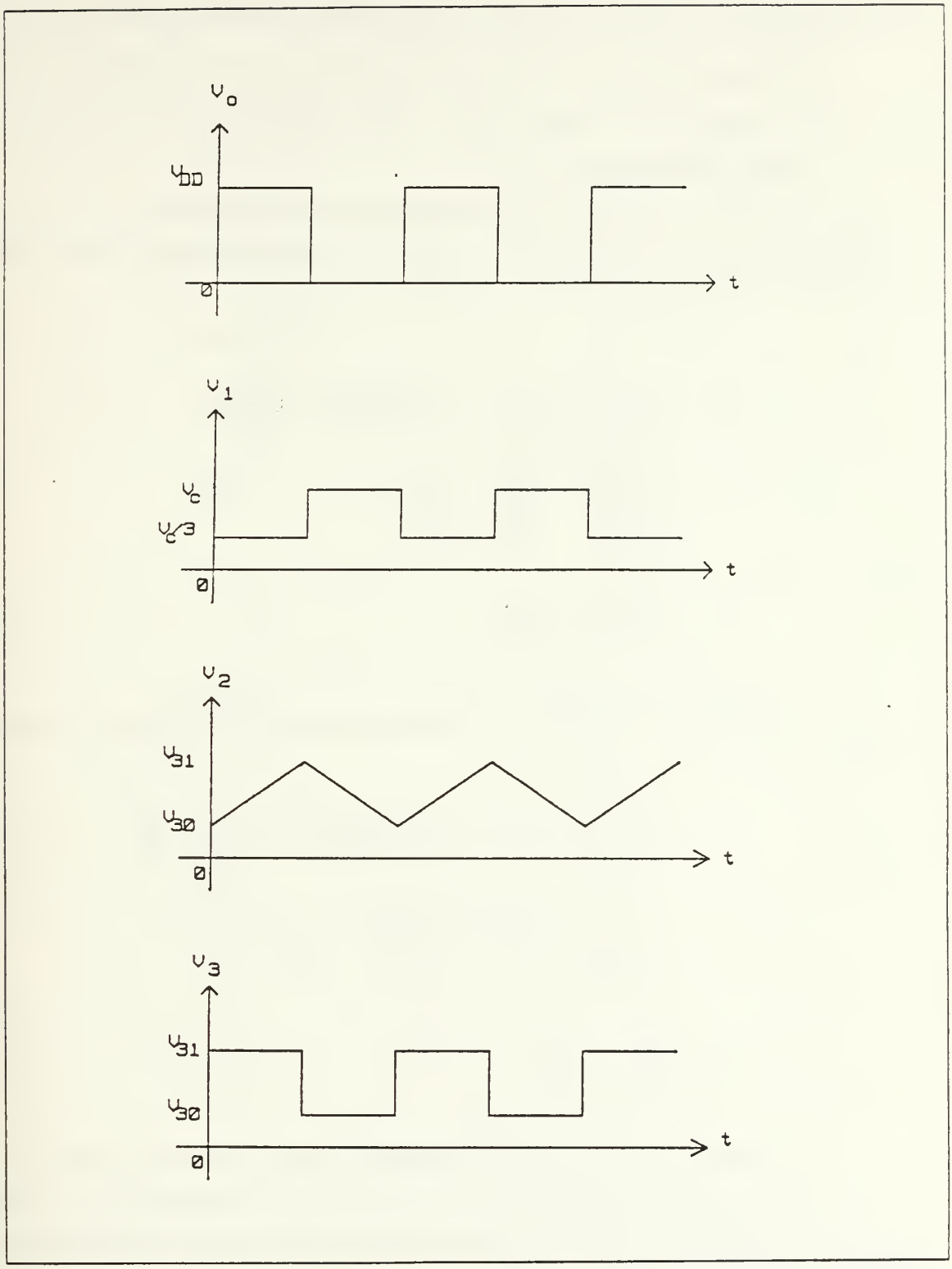

Figure 3.3 The Waveforms of the VCO.

produces a hysteresis which is a key behavior of the VCO operation. As v_0 changes between two values, so does the comparator (+) terminal voltage, v_3. If it did not change as the ramp voltage changed, it would immediately cause the comparator to change again. This would eliminate any control of the output signal frequency by VC.

To obtain a formula for the frequency of the VCO related to the input control voltage V_c, let us consider the positive ramp case, rising integrator. In Figure 3.4(b)., the output voltage v_2 is given as

$$v_2 = -\frac{1}{CR\,3}\int \frac{V_c}{3}\,dt + \mathcal{L}^{-1}\left[\frac{V_c/2}{s}\left[1+\frac{3}{sRC}\right]\right]$$

$$v_2 = -\frac{V_c}{RC}\,t + \frac{V_c}{2} + \frac{3V_c}{2RC}\,t$$

$$v_2 = \frac{V_c}{2}\left[\,1+\frac{t}{RC}\,\right] \qquad (3.3)$$

In the negative ramp case, the falling integrator of Figure 3.4(c), the output voltage v_2 is given as

$$v_2 = -\frac{1}{RC}\int V_c\,dt + \mathcal{L}^{-1}\left[\frac{V_c/2}{s}\left[\,1+\frac{1}{sRC}\,\right]\right]$$

$$v_2 = -\frac{V_c}{RC}\,t + \frac{V_c}{2} + \frac{V_c/2}{RC}\,t$$

$$v_2 = \frac{V_c}{2}\left[\,1-\frac{t}{RC}\,\right] \qquad (3.4)$$

If the graph of v_2 is drawn for the falling integrator case, because the slopes of both cases are the same, in Figure 3.5, the graph can be limited by the v_3 voltage values of the comparator which are given by Equations 3.1 and 3.2. These hysteresis limits give the graph a triangular shape.

$$v_2 = \frac{V_c}{2} - \frac{V_c}{2}\,\frac{t}{RC}$$

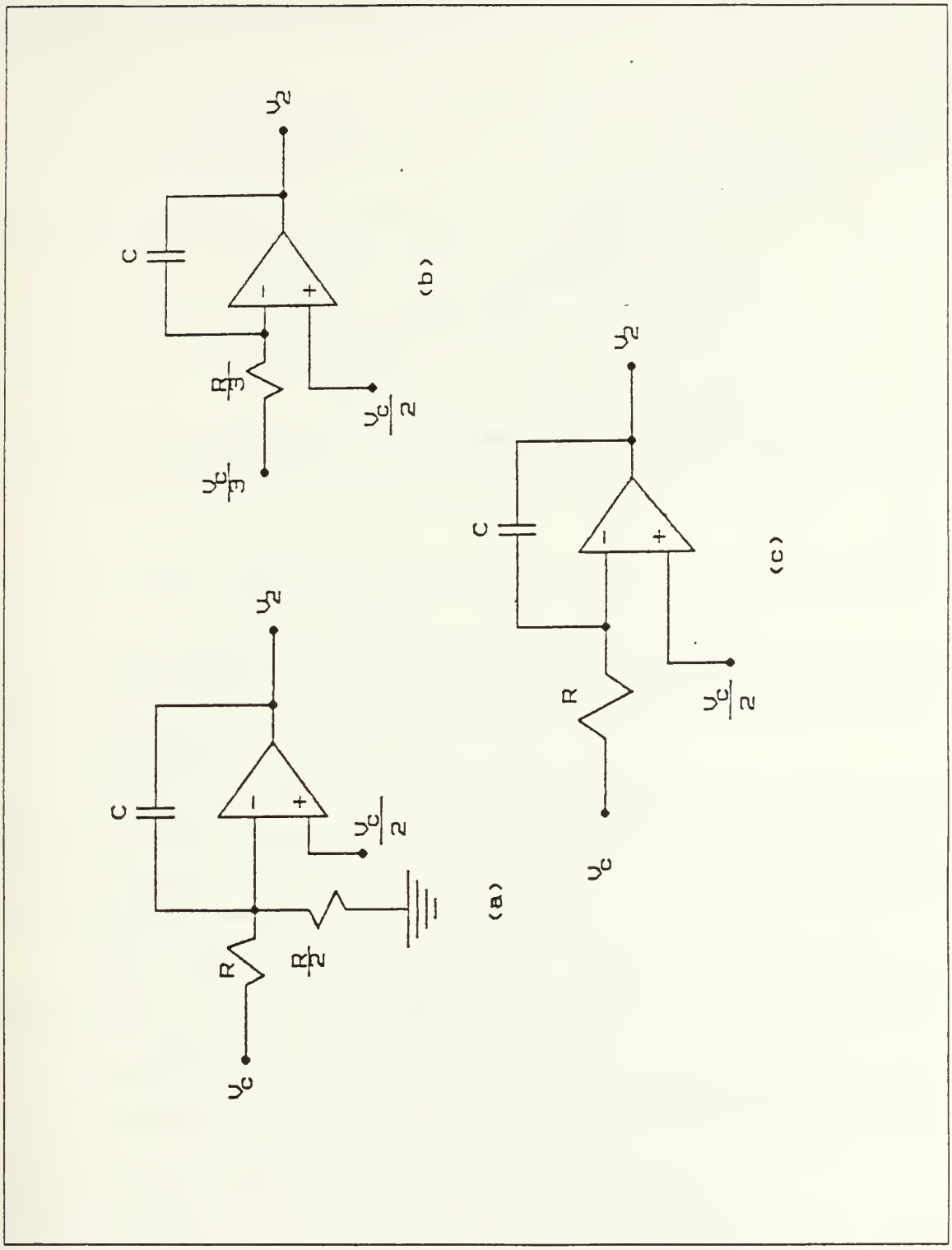

Figure 3.4 (a) Rising Integrator (b) Thevenin Equivalent circuit (c) Falling Integrator.

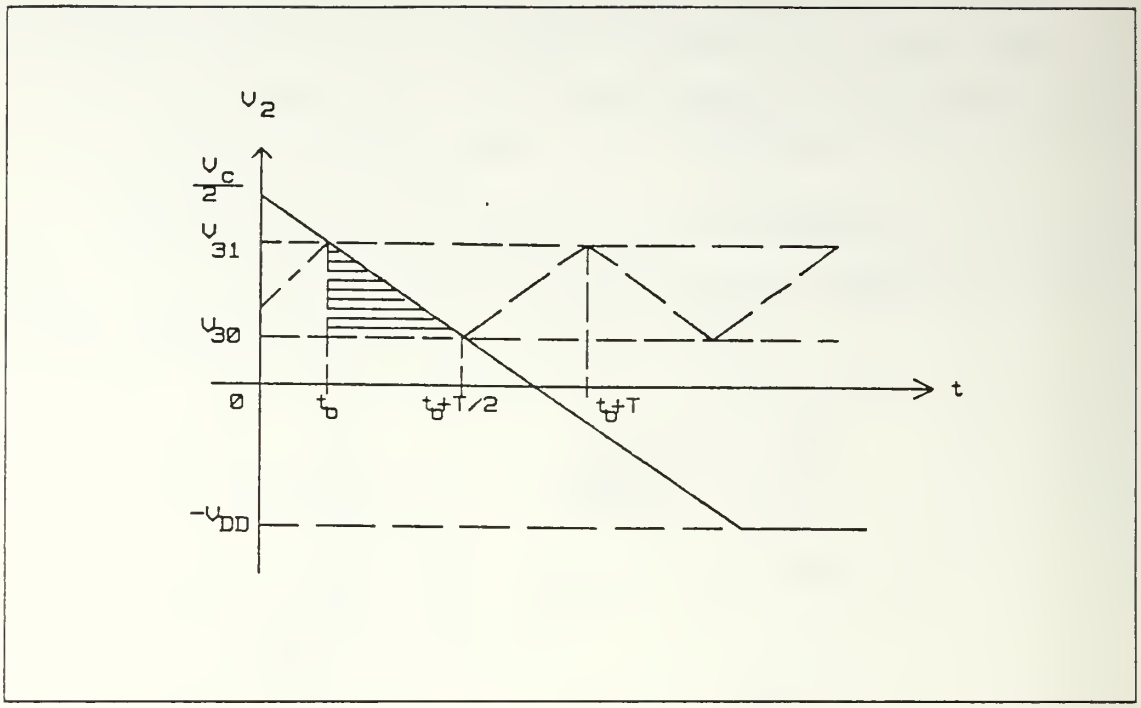

Figure 3.5 Falling Integrator Waveform of Figure 3.4(c).

when $t = t_0$

$$v_2 = v_{31} = \frac{V_c}{2} - \frac{V_c}{2}\frac{t_0}{RC} \tag{3.5}$$

when $t = t_0 + T_c/2$;

$$v_2 = v_{30} = \frac{V_c}{2} - \frac{V_c}{2}\frac{(t_0 + T_c/2)}{RC} \tag{3.6}$$

If Equation 3.6 is substracted from Equation 3.5

$$v_{31} - v_{30} = \frac{V_c}{4}\frac{T_c}{RC} \tag{3.7}$$

The period of the triangular wave which is also the period of the VCO output can be obtained as

$$T_c = \frac{4RC(v_{31}-v_{30})}{V_c} \tag{3.8}$$

The frequency can also be found as

$$f_c = \frac{V_c}{4RC(v_{31}-v_{30})} \tag{3.9}$$

It can easily be seen that there is a linear relationship between the control voltage, V_c, and the output frequency of the VCO, f_c. The VCO sensitivity is defined as

$$K_3 = \frac{1}{4RC(v_{31}-v_{30})} \tag{3.10}$$

where the unity of K_3 is Hz Volt or rad/s Volt. The experimental results showed that longer integrator outputs result in a decrease in the linearity of the VCO.

2. **Phase Detector**

Generally, there are two categories for phase detectors, sinusoidal signal phase detectors and square signal phase detectors, [Ref. 6]. In the square case, the signal may be the original waveform of the signals used or may have been produced by hard limiting followed by amplification of sinusoidal signals.

The advantage of the square signal phase detectors is that the output of the phase detector is independent of the input voltage levels, eliminating the automatic gain control requirement. The other important advantage is that the sensitivity K_1 of the sinusoidal phase detectors is not constant within an interval $(0,\pi)$ or formed of truncated sinusoids. However, when the signals involved are square waves, or when it is possible to transform them into square waves, phase detectors featuring a linear characteristic over a certain interval are fairly easy to construct.

In Figure 3.6(a) the EXCLUSIVE-OR output signal can be used as a linear phase detector, resulting 0 when signals e'_s and e_R have the same sign, and 1 otherwise. The network implements the function

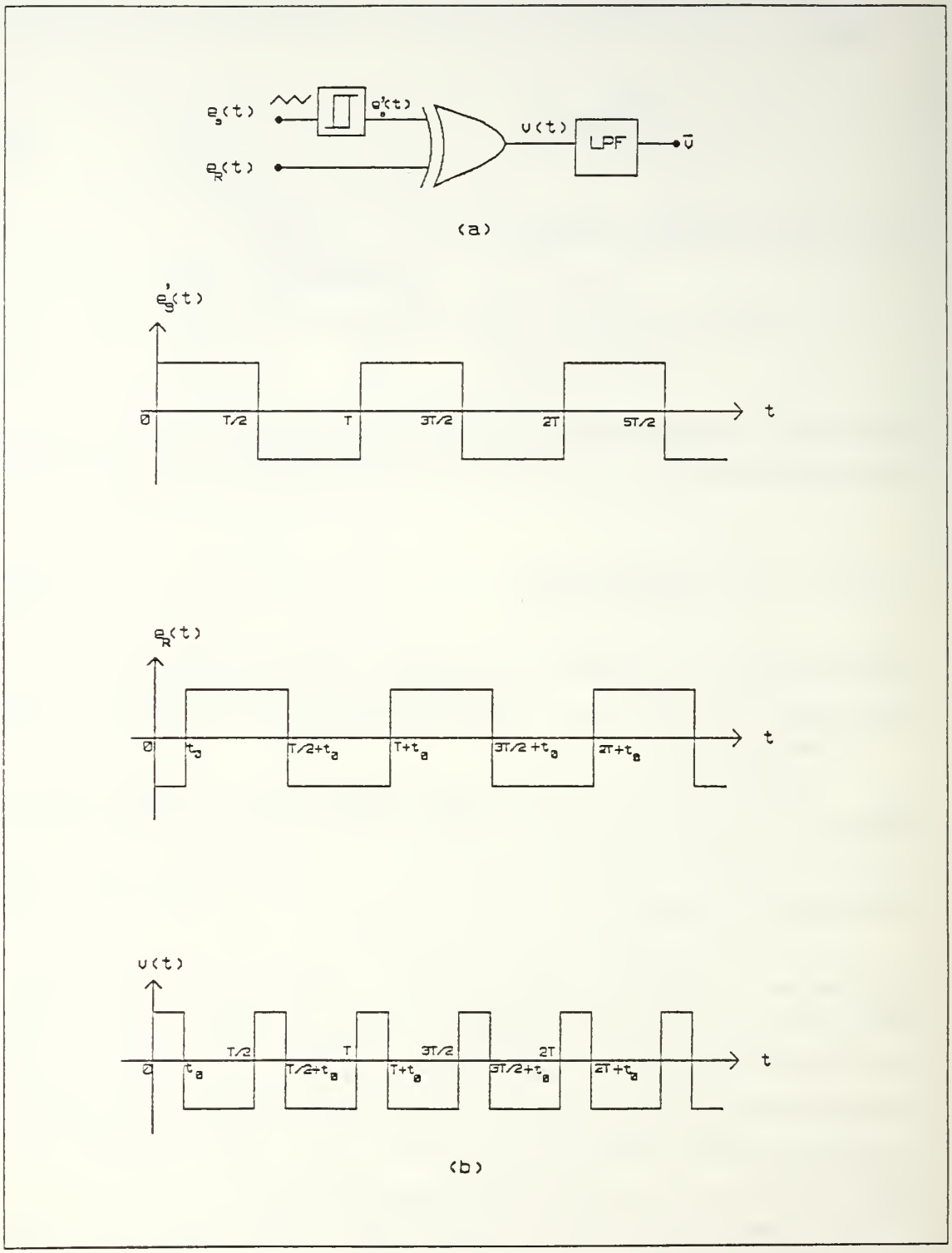

Figure 3.6 (a)XOR and LP Circuit for a Square Signal Phase Detection
(b)Input and Output Waveforms of XOR Operation.

$$v(t) = A\ \mathrm{Sign}[e'_s] \oplus \mathrm{Sign}[e_R] \qquad (3.11)$$

If the v(t) signal dc component v is extracted by low-pass filtering, the value of the dc component of the signal v(t) can be calculated as a function of the phase difference, $\Phi = \Phi_i - \Phi_o$, Φ_i representing the input signal phase, and Φ_o representing the VCO output signal phase

$$\bar{v} = \frac{1}{T}\int_0^T v(t)\,dt$$

when $0 < \Phi < \pi$

$$\bar{v} = \frac{A}{T}\left[\int_0^{t_0} dt + \int_{t_0}^{T/2} -dt + \int_{T/2}^{T/2+t_0} dt + \int_{T/2+t_0}^{T} -dt\right]$$

$$\bar{v} = \frac{A}{T}(4t_0 - T)$$

$$\bar{v} = \frac{2A}{T}\left(2t_0 - \frac{T}{2}\right)$$

$$\bar{v} = \frac{2A}{\pi}\left(\Phi - \frac{\pi}{2}\right) \qquad \text{for } 0 \le \Phi < \pi \qquad (3.12)$$

where $\Phi = (t_0/T)\,2\pi$. The corresponding characteristic is represented in Figure 3.7. The phase detector sensitivity value is

$$K_1 = \left|\frac{dv}{d\Phi}\right| = \frac{2A}{\pi} \qquad (3.13)$$

The characteristic can be made independent of signal $e_s(t)$ amplitude by including a limiter in the circuit preceding the phase detector. This implementation is also shown in Figure 3.6(a). Therefore it can finally be said that the phase detector sensivity depends only on the logic voltage levels.

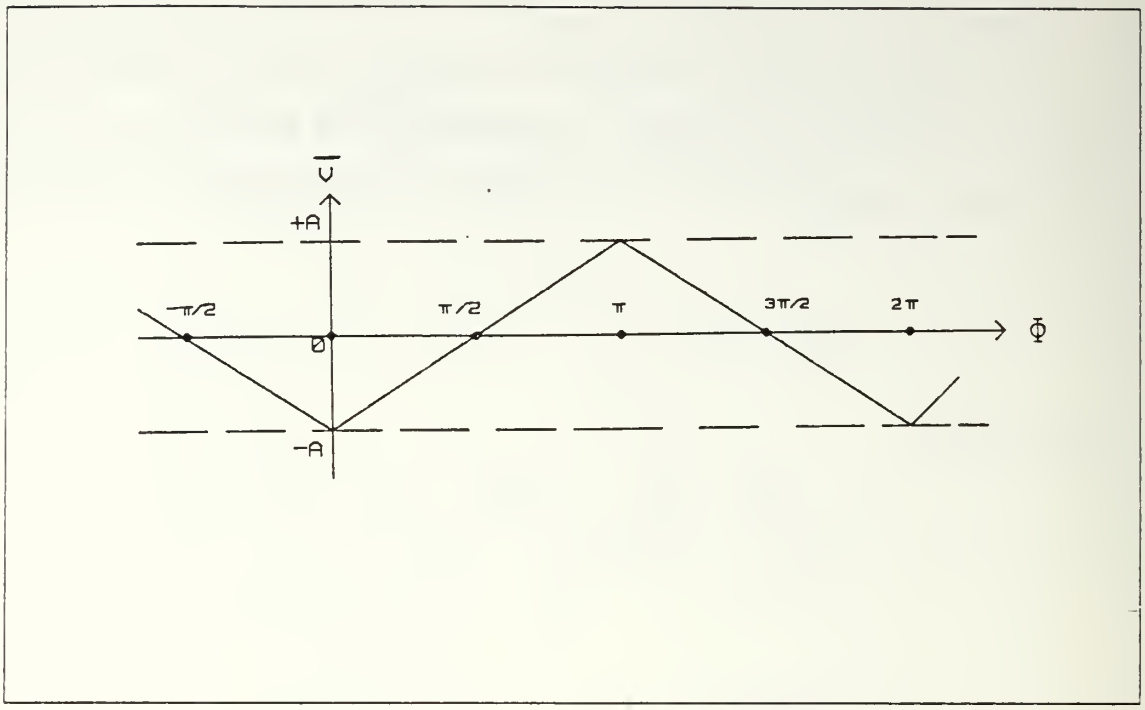

Figure 3.7 Characteristic of the EXCLUSIVE-OR Logic Circuit of Figure 3.6(a).

3. **Loop Filter**

Loop filters are lowpass filters that are set between the phase detector output and the amplifier input. The transfer function of the loop filter has a considerable influence on the properties of the loop. The simplest low-pass filter to construct is the RC filter of the transfer function

$$F(s) = \frac{1}{1 + s\tau_1} \tag{3.14}$$

where τ_1 = RC. The implementation of this transfer function is shown in Figure 3.8(a). The use of such a filter produces a second-order loop. However, the performances obtained are relatively restricted, mainly because only one parameter is involved, the time constant τ_1. This prevents an independent choice of the two essential parameters of a second-order loop, namely the natural angular frequency, w_n, and the damping factor, ζ, when the loop gain K is otherwise given.

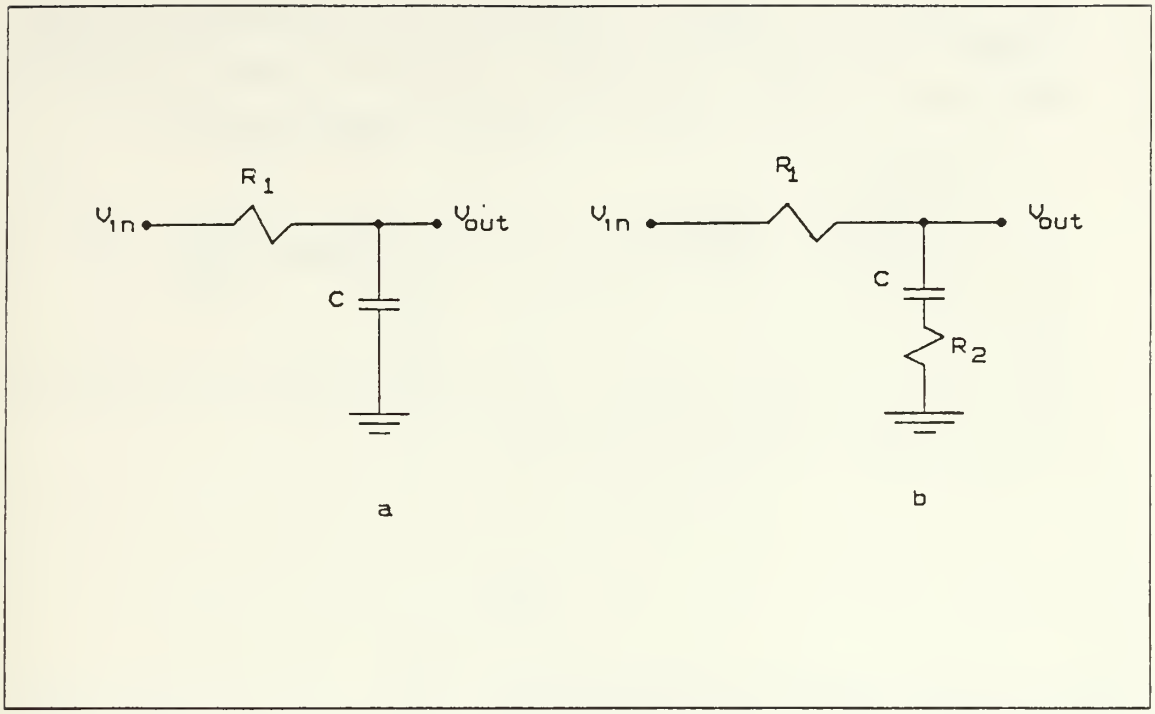

Figure 3.8 (a) One-pole Low-Pass Filter
(b) One-pole Low-Pass Filter With Phase-lead Correction Network.

If a resistor is added in series with the capacitor of the filter, C, the required additional parameter can be obtained. This configuration in Figure 3.8(b) is called phase-lead correction network, [Ref. 6], and the transfer function of the filter is

$$F(s) = \frac{1+s\tau_2}{1+s\tau_1} \tag{3.15}$$

where $\tau_2 = R_2C$ and $\tau_1 = (R_1 + R_2)C$. By judicious choice of elements R_1, R_2 and C, the time constants τ_1 and τ_2 can be obtained independently

4. **Loop Amplifier**

In some cases, a gain amplifier K_2 has to be fitted between the phase detector and the VCO. This is, in particular, the case when the phase detector sensitivity K_1 and the VCO modulation sensitivity K_3 are not high enough to produce a given loop gain K. The use of gain amplifier K_2 overcomes this difficulty, since the loop gain K then becomes

$$K = K_1 K_2 K_3 \tag{3.16}$$

The implementation in Figure 3.9 was used in the PLL as a hardware application. The amplifier is an inverting type amplifier. The reason of using an inverting amplifier comes from the stability conditions of the PLL. The gain is given as

$$K_2 = -\frac{R_f}{R} \tag{3.17}$$

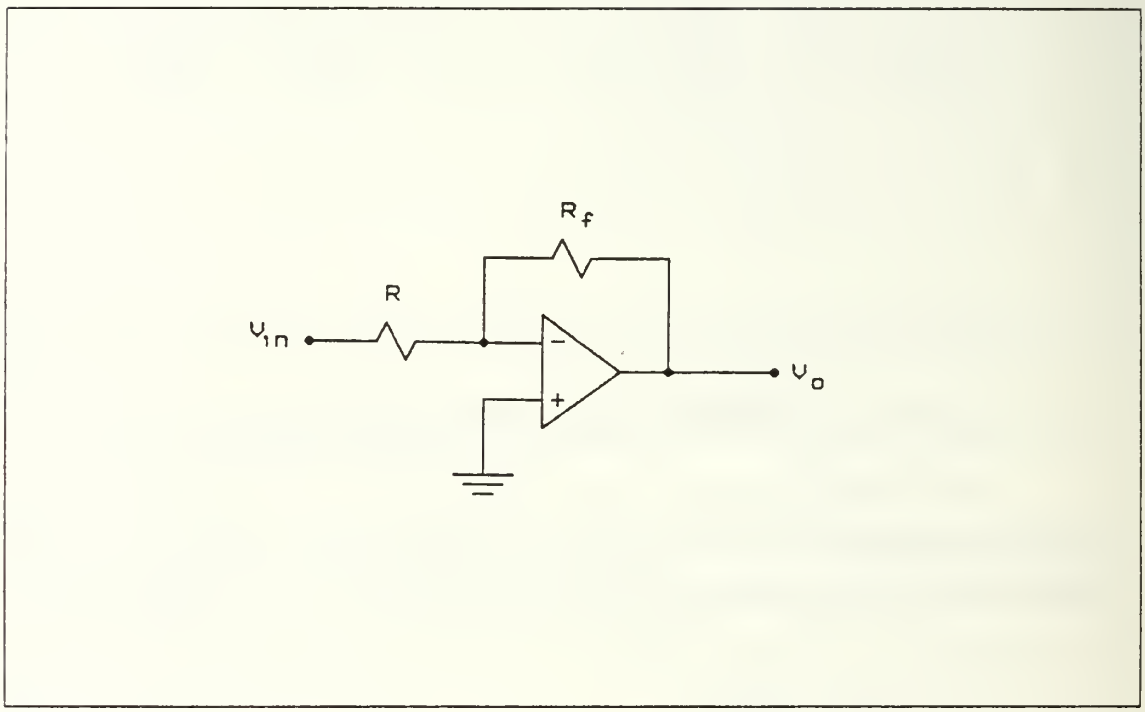

Figure 3.9 Amplifier for the PLL.

B. GENERAL EQUATIONS

The phase-locked loop represented in Figure 3.10 is a device by means of which a voltage controlled oscillator (VCO) delivers an output signal y_o, in synchronism with the input signal y_i. The input signal is obtained by passing the actual input waveform through a hard limiter. As mentioned before, this will produce a linearly behavioured PLL.

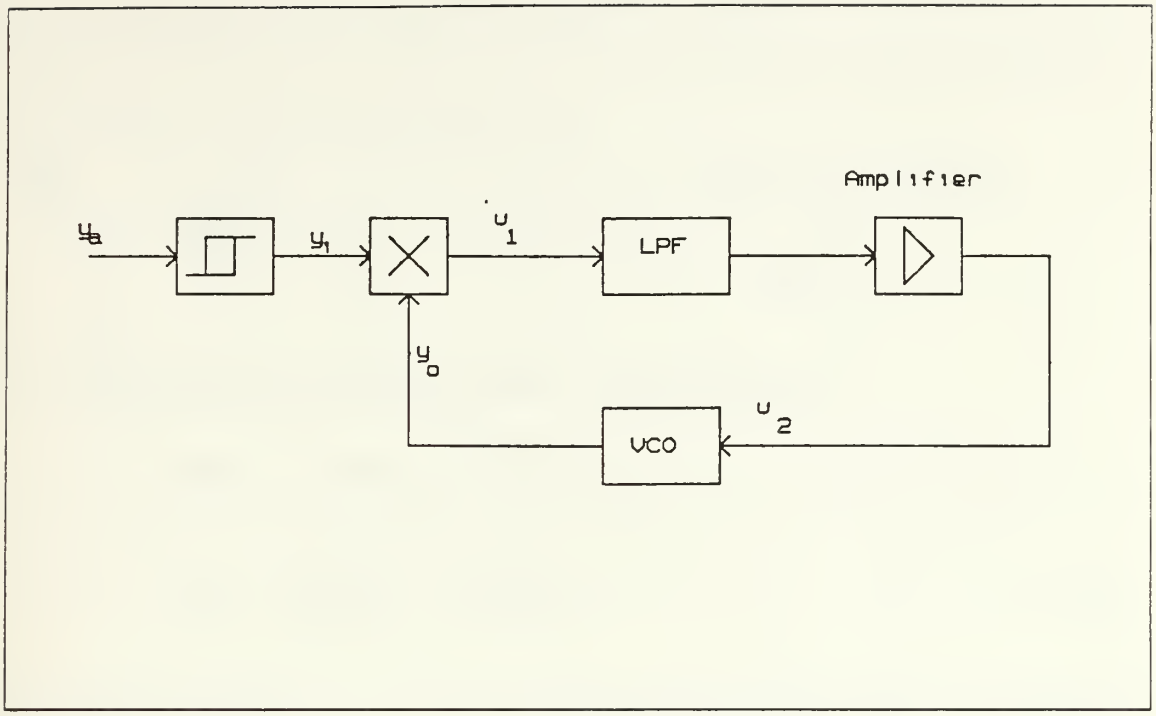

Figure 3.10 Block Diagram of a Phase-Locked Loop.

1. **General Time Domain Equations**

In the diagram shown in Figure 3.2, the input signal y_i and VCO output signal y_o are expressed as

$$y_a(t) = A'\sin[wt + \Phi_i(t)]$$

$$y_i(t) = A\text{Sign}[\sin[wt + \Phi_i(t)]]$$

$$y_o(t) = A\text{Sign}[\sin[wt + \Phi_o(t)]]$$

These signals have not necessarily the same angular frequency, the difference can easily be included in $\Phi_i(t)$ - $\Phi_o(t)$. The output signal results from the XOR operation

$$A\text{Sign}[\sin[wt + \Phi_i(t)]] \oplus \text{Sign}[\sin[wt + \Phi_o(t)]] \qquad (3.18)$$

From Figure 3.11 the intermediate signals can be defined as

$$u_1(t) = K_1[\Phi_i(t) - \Phi_o(t)] \qquad (3.19)$$

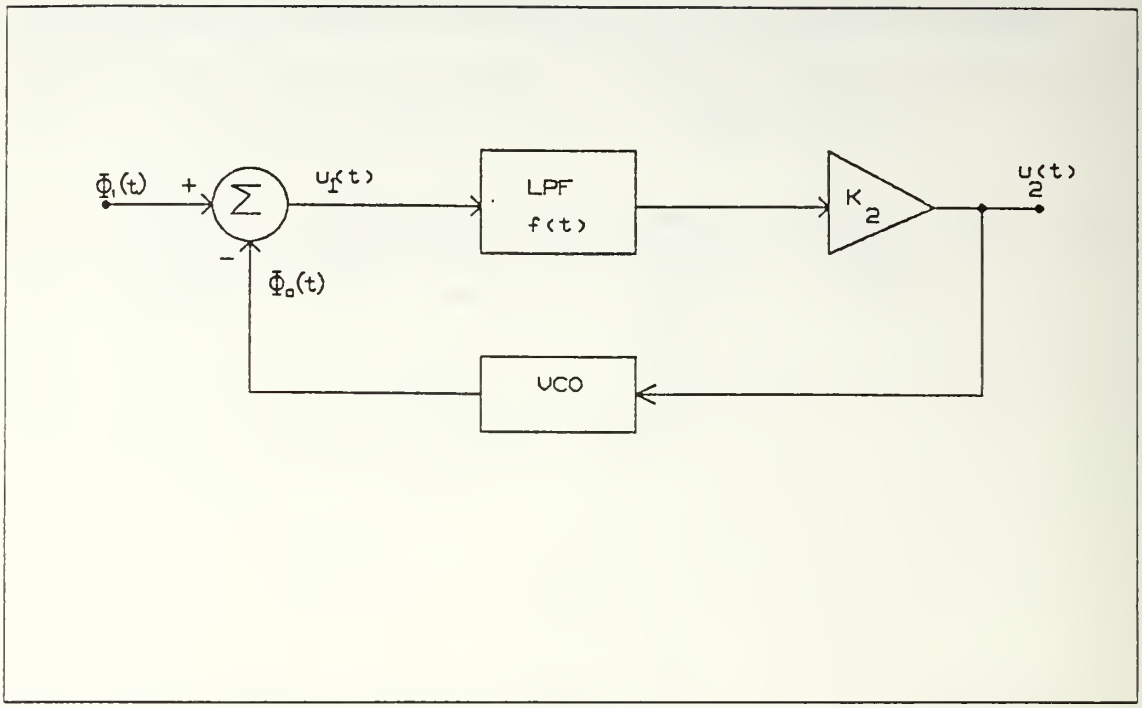

Figure 3.11 Linear Model of the PLL.

where $K_1 = 2A/\pi$. If F(s) is the loop filter transfer function given by Equation 3.15 and f(t), its impulse response, the control signal of the VCO is given as

$$u_2(t) = K_2\, u_1(t) * f(t) \tag{3.20}$$

The symbol * represent the convolution product. Finally, since the VCO is a frequency-modulated oscillator, K_3 being its modulation sensivity in rad/sec/volt,

$$\frac{d\Phi}{dt} = K_3 u_2(t) \tag{3.21}$$

If Equation 3.19, Equation 3.20, and Equation 3.21 are combined, general time-domain equation that governs the behaviour of PLL can be obtained as

$$\frac{d\Phi_o}{dt} = K_1 K_2 K_3 \left[\Phi_i(t) - \Phi_o(t) \right] * f(t) \tag{3.22}$$

The product $K_1K_2K_3$ is replaced by $K = K_1K_2K_3$. The constant K then represents the servo device open-loop gain. To supply the negative sign to the summation, one of the constants, K_1, K_2, K_3, should be negative. Hence, a stable PLL can be obtained. The general equation is thus

$$\frac{d\Phi_o}{dt} = K [\Phi_i(t) - \Phi_o(t)] * f(t) \tag{3.23}$$

If the Laplace transform is used, the general equation becomes

$$s\Phi_o(s) = K [\Phi_i(s) - \Phi_o(s)] F(s)$$

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{KF(s)}{s + KF(s)} \tag{3.24}$$

The quantity $\Phi(s)\ \Phi_i(s) = 1 - H(s)$ is the error function of the PLL, where $\Phi(t)$ is the instantaneous phase error given by

$$\Phi(t) = \Phi_i(t) - \Phi_o(t)$$

The error function is given by

$$1 - H(s) = \frac{\Phi(s)}{\Phi_i(s)} = \frac{s}{s + KF(s)} \tag{3.25}$$

The corresponding loop filter transfer function is given by Equation 3.15. If Equation 3.15 is inserted in Equation 3.24 and Equation 3.25, the transfer and error function equations can be obtained as

$$H(s) = \frac{K\tau_2 s + K}{\tau_1 s^2 + (1 + K\tau_2)s + K} \tag{3.26}$$

$$1 - H(s) = \frac{\tau_1 s^2 + s}{\tau_1 s^2 + (1 + K\tau_2)s + K} \tag{3.27}$$

Using Equation 3.26 and Equation 3.27, the equations corresponding to the time domain can easily be derived.

$$\tau_1 \frac{d^2\Phi_o}{dt^2} + (1 + K\tau_2)\frac{d\Phi_o}{dt} + K\Phi_o(t) = K\tau_2\frac{d\Phi_i}{dt} + K\Phi_i(t) \tag{3.28}$$

$$\tau_1 \frac{d^2\Phi}{dt^2} + (1 + K\tau_2)\frac{d\Phi}{dt} + K\Phi(t) = \tau_1 \frac{d^2\Phi_i}{dt^2} + \frac{d\Phi_i}{dt} \tag{3.29}$$

2. **Parameters of a Second Order Loop**

The denominator of the second order transfer and error functions, when Laplace transformation is used, is generally formulated as $s^2 + 2\zeta w_n s + w_n^2$, where w_n is the natural angular frequency and ζ is the damping factor. It is stated, by definition,

$$w_n^2 = \frac{K}{\tau_1} \tag{3.30}$$

$$2w_n\zeta = \frac{1 + K\tau_2}{\tau_1} \tag{3.31}$$

The advantage of using one-pole low-pass filter with phase lead correction as the loop filter becomes more clear if Equation 3.30 and Equation 3.31 are considered; the natural angular frequency, w_n, can easily be controlled by changing τ_1, and the damping factor, ζ, can be controlled by changing τ_2 independently. With these notations, the quantity $K(\tau_2/\tau_1)$ can be expressed

$$K\frac{\tau_2}{\tau_1} = 2\zeta w_n - \frac{1}{\tau_1} = 2\zeta w_n - \frac{w_n^2}{K} \tag{3.32}$$

The transfer and error functions, Equations 3.26 and 3.27 respectively, become

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{(2\zeta w_n - w_n^2/K)s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \tag{3.33}$$

$$1 - H(s) = \frac{\Phi(s)}{\Phi_i(s)} \frac{s^2 + (w_n^2 K)s}{s^2 + 2\zeta w_n s + w_n^2} \tag{3.34}$$

C. TRANSIENT RESPONSE

In this section the response of the loop to different disturbances occuring at instant t=0 will be examined. The disturbances involved are

* Input signal phase step θ
* Input signal angular frequency step Δw

1. Phase Step Response

At instant t = 0, a θ amplitude phase step is applied to the input signal

$$\Phi_i(t) = \theta\, \gamma(t) \tag{3.35}$$

where $\gamma(t)$ is the unit step function. In Laplace Transformation form

$$\Phi_i(s) = \frac{\theta}{s} \tag{3.36}$$

the phase step response of the VCO can be obtained using Equation 3.33 and Equation 3.36.

$$\Phi_o(s) = \frac{[(2\zeta w_n - w_n^2 K)s + w_n^2]\theta / s}{s^2 + 2\zeta w_n s + w_n^2} \tag{3.37}$$

also the phase error, $\Phi(s) = \Phi_i(s) - \Phi_o(s)$, can be derived

$$\Phi(s) = [\, 1 - H(s)\,] \frac{\theta}{s} \tag{3.38}$$

This leads to

$$\Phi(s) = \frac{(s + w_n^2 K)\theta}{s^2 + 2\zeta w_n s + w_n^2} \tag{3.39}$$

2. **Frequency Step Response**

If a frequency step Δw is applied to the input signal at instant $t = 0$

$$\Phi_i(t) = \Delta w \, t \, \gamma(t) \tag{3.40}$$

In Laplace transformation form

$$\Phi_i(s) = \frac{\Delta w}{s^2} \tag{3.41}$$

The frequency step response of the error function using Equation 3.34 and Equation 3.41 is given by

$$\Phi(s) = [\, 1 - H(s) \,] \frac{\Delta w}{s^2} \tag{3.42}$$

this also leads to

$$\Phi(s) = \frac{\Delta w}{s^2 + 2\zeta w_n s + w_n^{\,2}} + \frac{w_n^{\,2}}{K} \frac{\Delta w}{s(s^2 + 2\zeta w_n s + w_n^{\,2})} \tag{3.43}$$

D. EXPERIMENTAL RESULTS OF THE ANALOG PLL

Using the derived functions in the previous sections, a prototype analog phase-locked loop was implemented in hardware. This implementation was converted to a switched-capacitor realization of the PLL. Prior to the SC implementation the experimental results have been recorded to compare the analog and the SC versions of the PLL.

1. **Voltage Controlled Oscillator (VCO)**

It is very important to build a linear VCO in some PLL applications. However, a tolerance of 5% or 10% on the linearity of the modulation characteristic within the frequency variation range is more often than not acceptable, except for certain applications, such as the use of a phase-locked loop as a good linear frequency discriminator.

The circuit in Figure 3.12 was built in prototype, and voltage frequency relation is given in Figure 3.13. The dotted line in Figure 3.13 is drawn according to Equation 3.9.

$R = 10\ K\Omega$

$C = 730\ pF$

$v_{31} - v_{30} = 1.2\ V$ (from Figure 3.14)

The waveforms of the VCO are given in Figure 3.14. To make the triangular wave of the integrator in Figure 3.12 short, two comparators were used. The output voltage levels of the first comparator were (+6.5,0) volts and the second comparator output voltage levels were (+6.5,-6.5) volts. The second comparator also provided the logic levels for the XOR operations.

2. **Loop Behavior**

To construct the phase-locked loop, the configuration in Figure 3.15 was used. The input to the PLL can be any periodic waveform. This input is converted to a square waveform by a zero-crossing comparator. At the same time, the logic level adjustment for the XOR operation is done. The other input of the XOR comes from a frequency divider. For this purpose a digital counter was used. The clock input of the counter is fed by the VCO output. Any of the outputs of the counter can be used as the input to the XOR. If Q_1 is used, the VCO frequency is divided by 2, if Q_2 is used, the VCO frequency is divided by 4, if Q_3 is used, the VCO frequency is divided by 8, and so on. At the same time, integer multiples of the input frequency can be obtained when the PLL is in lock. For instance, if Q_3 is used as an output from the counter, The Q_2, Q_1, and the VCO output are integer multiples of the input frequency by 2, 4, and 8 respectively.

In the experiment an LF356N CMOS operational amplifier was used as the loop amplifier. The gain K_2 was 5.1. This operational amplifier was also used as a summer to obtain a free running frequency for the VCO. Since it was an inverting summer, the acquisition voltage was obtained from the negative power supply. The 18 KΩ resistance can be changed to obtain a different free-running frequency of the VCO. VCO control voltage, V_c, can vary between 0 V and $2(V_{DD}-1.5V)$ and provides a wide range of frequencies. The power supplies used in the prototype are (+6.5,-6.5)V, so V_c can vary between 0 V and 10 V. Since this control voltage is obtained from the amplifier and the saturation voltage of the operation amplifier is 5V, the control

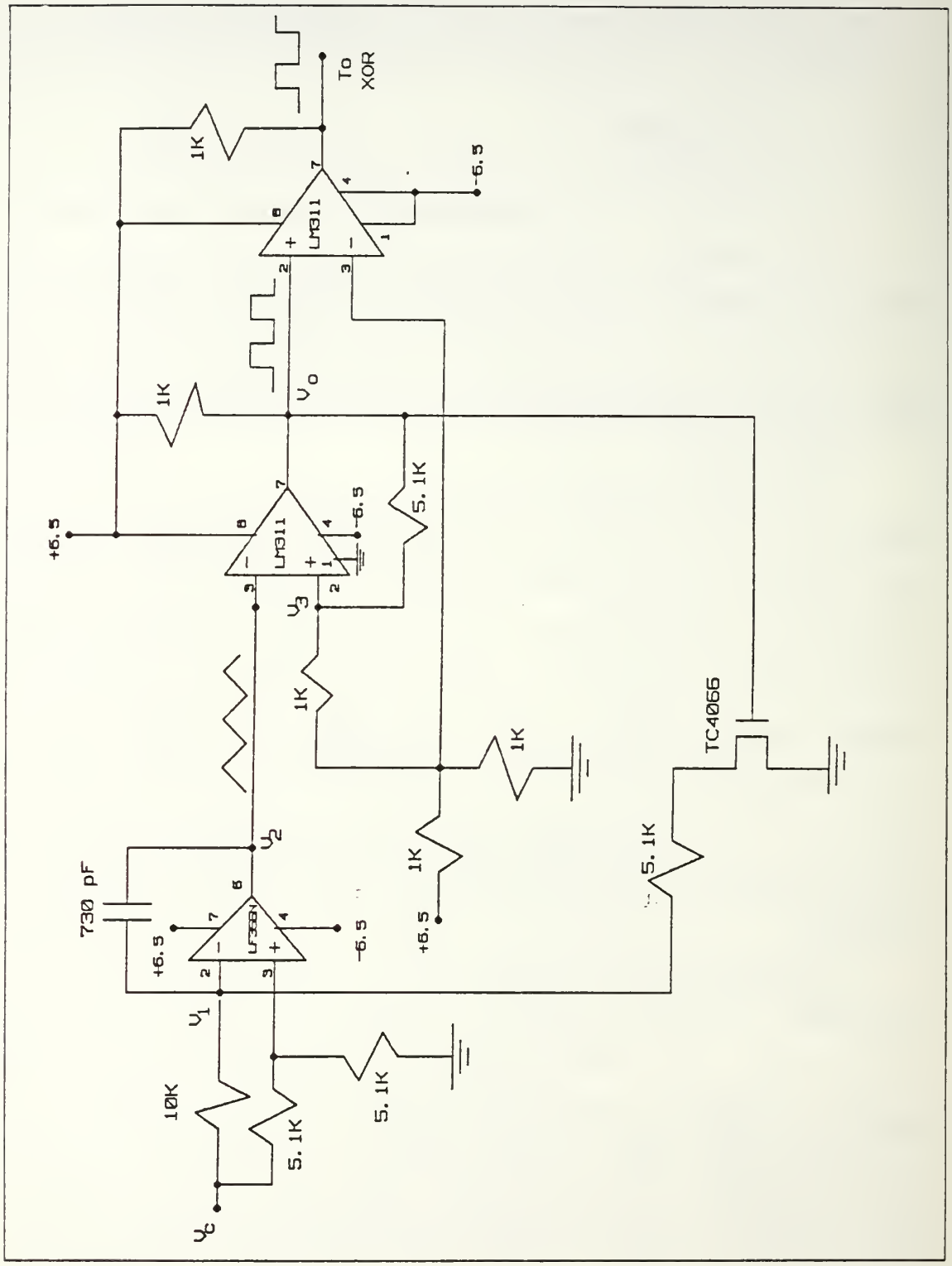

Figure 3.12 Prototype Voltage Controlled Oscillator VCO.

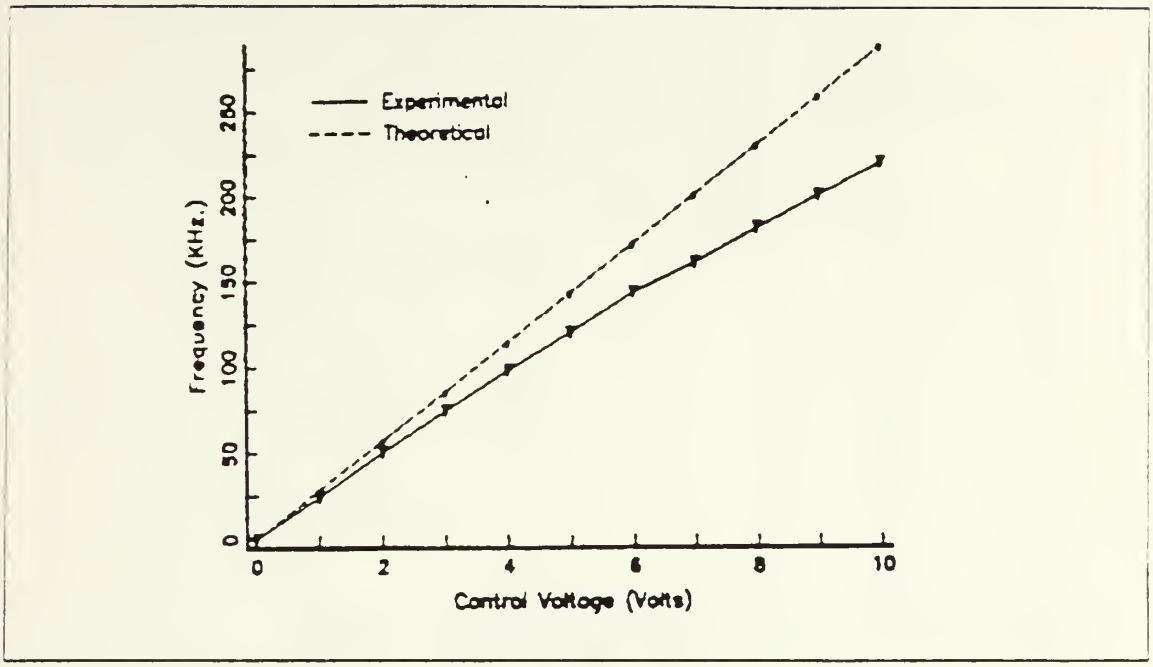

Figure 3.13 VCO Frequency-Voltage Relationship.

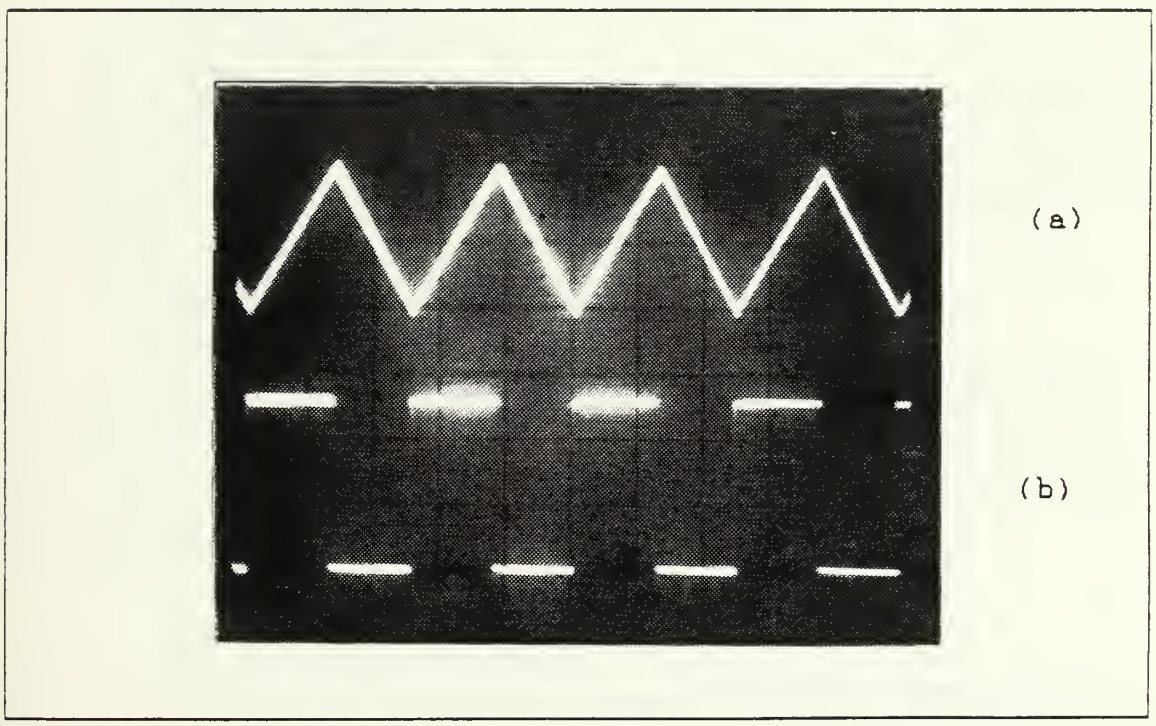

Figure 3.14 (a) The Output of the Integrator (0.5 volt/div.)
(b) The Output of the VCO (5 volt/div, 5 μsec/div).

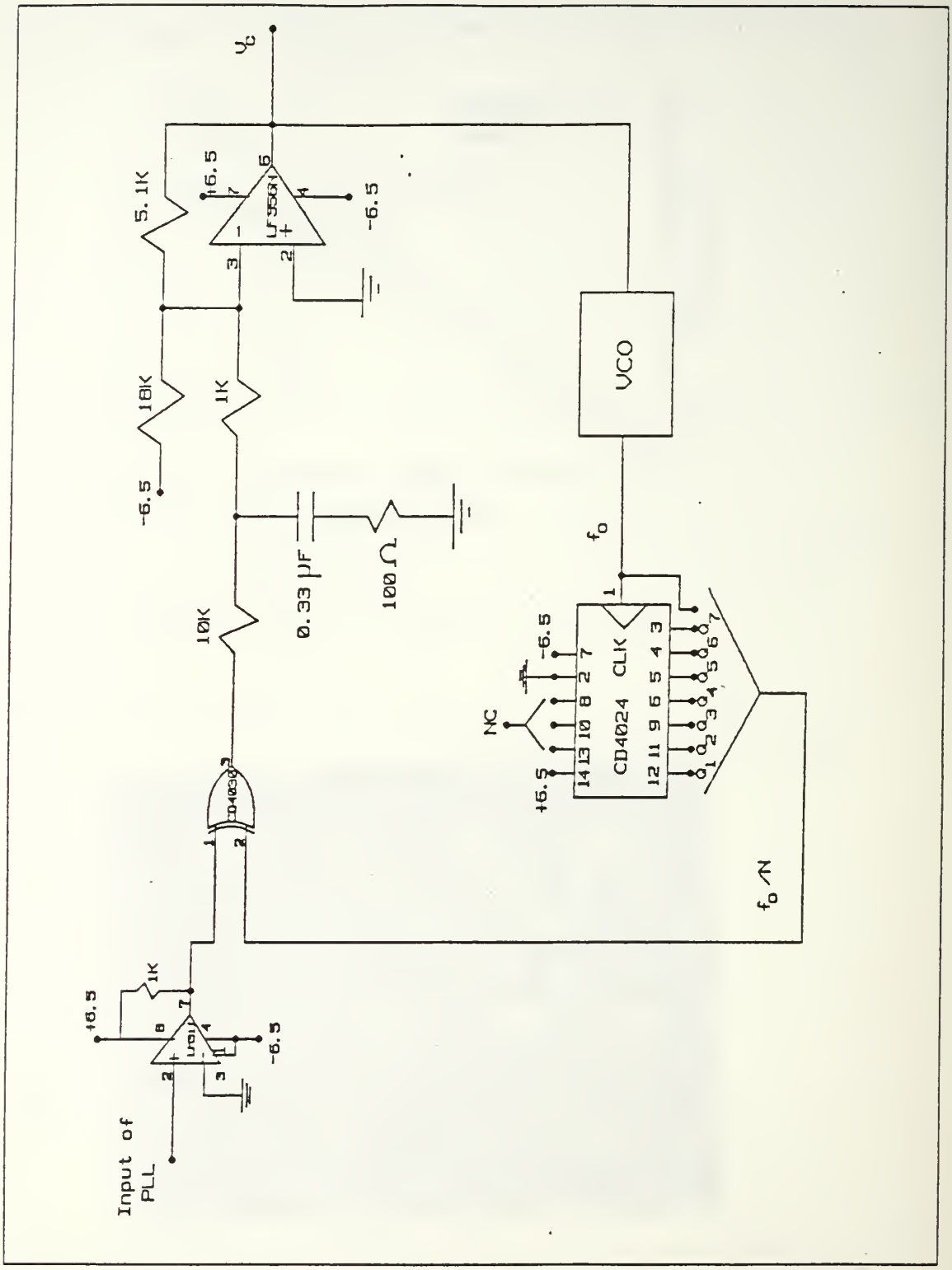

Figure 3.15 The Prototype Phase-Locked Loop.

voltage cannot exceed 5V. The other concern is the loop gain K. Since the amplifier is an inverting type amplifier, this provides the required negative constant for stability and supplies a positive control voltage to the VCO for proper operation.

As the loop filter, a single-pole low-pass filter with phase lead correction was used. The time constants τ_1 and τ_2 in Equation 3.15 are given as

$$\tau_1 = (R_1 + R_2)C$$
$$\tau_1 = (10 \times 10^3 + 100)0.33 \times 10^{-6}$$
$$\tau_1 = 3.33 \text{ msec.}$$

which yields a pole frequency of 48 Hz. Also

$$\tau_2 = R_2C$$
$$\tau_2 = 100 \times 0.33 \times 10^{-6}$$
$$\tau_2 = 33 \ \mu\text{sec.}$$

and a zero frequency of 4.8 KHz. If these time constants are inserted into Equation 3.15, the transfer function of the loop filter is obtained as

$$F(s) = \frac{1 + 33. \times 10^{-6}s}{1 + 3.33 \times 10^{-3}s} \tag{3.44}$$

The frequency response of the loop filter is given in Figure 3.16 and the frequency response obtained from a digital signal processor, SD-360, is given in Figure 3.17. Referring to Figure 1.8, the capture and lock ranges were recorded as following

$$f_{cap} = 4.5 \text{ KHz.} - 65 \text{ KHz.}$$
$$f_{lock} = 4.5 \text{ KHz.} - 97 \text{ KHz.}$$

These results were obtained by connecting the VCO output directly to one of the XOR inputs. When the PLL was in lock, the input frequency was equal to the VCO frequency. Then, Q_1 output of the counter was connected to the XOR input. The corresponding capture and lock ranges were recorded as following

$$f_{cap} = 2.25 \text{ KHz.} - 32.5 \text{ KHz.}$$
$$f_{lock} = 2.25 \text{ KHz.} - 48.5 \text{ KHz.}$$

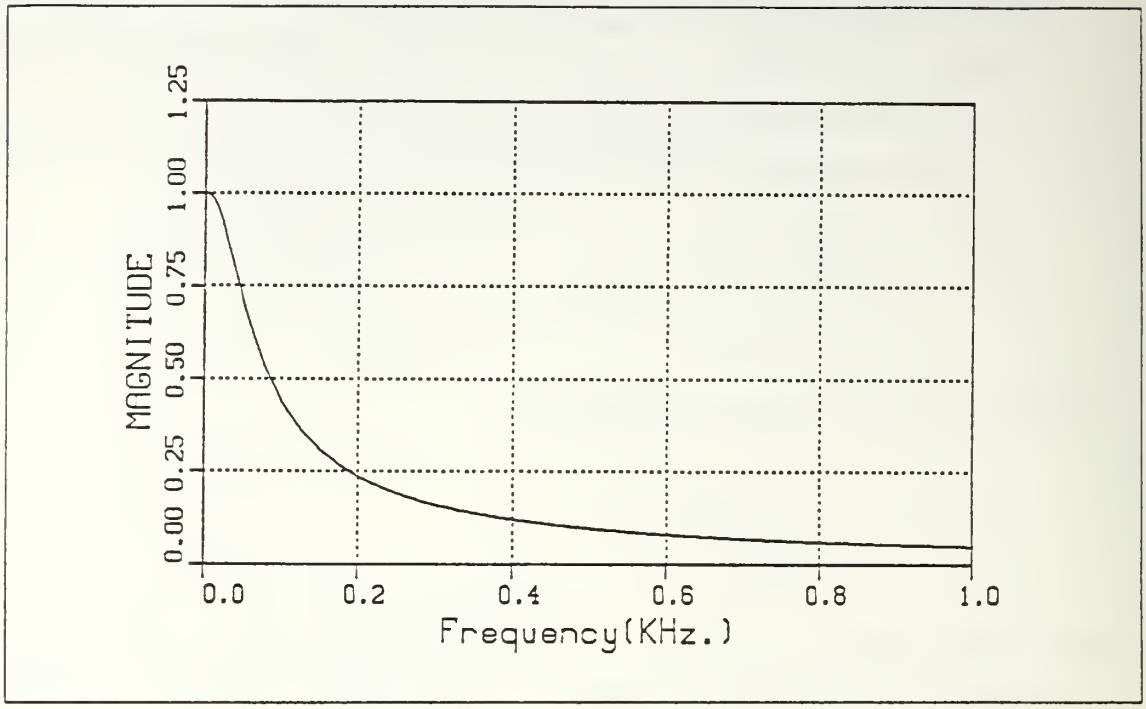

Figure 3.16 (a) Magnitude Response of the Loop Filter.

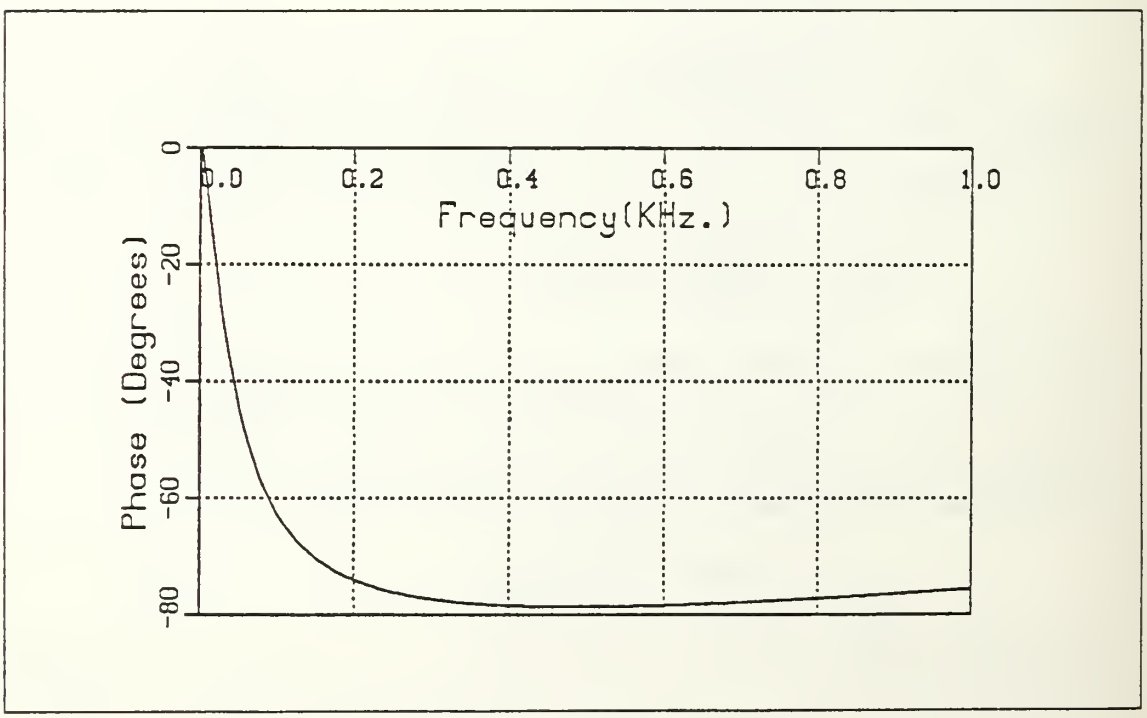

Figure 3.16 (b) Phase Response of the Loop Filter.

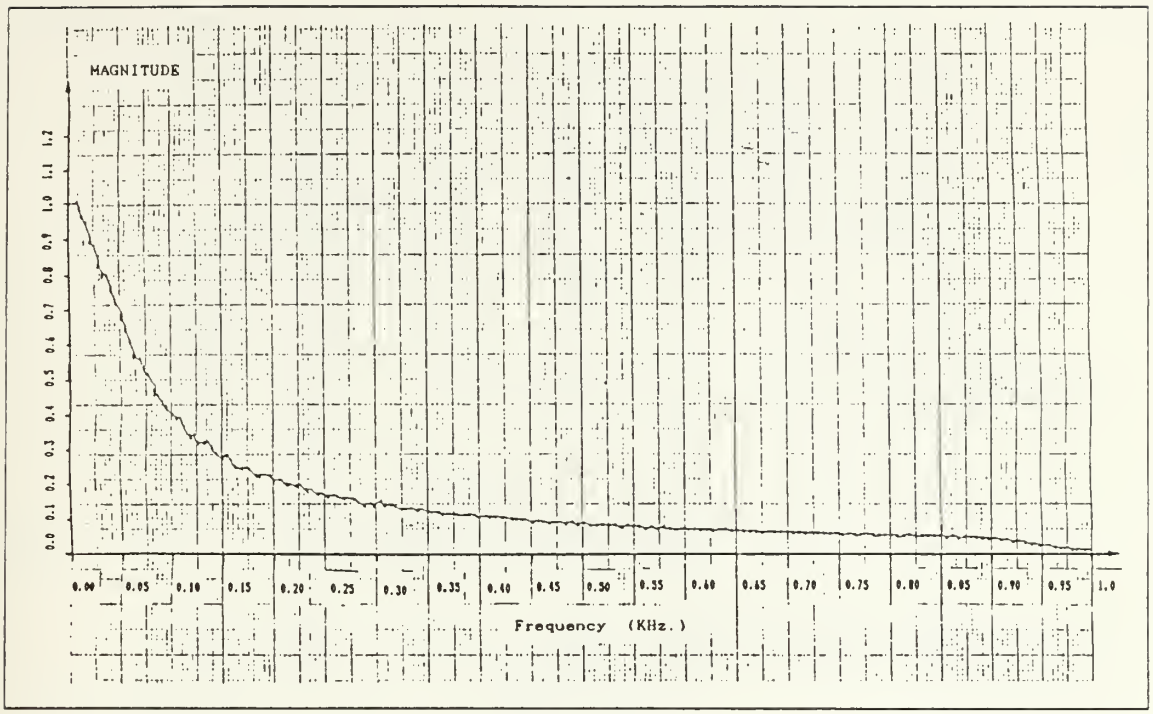

Figure 3.17 Frequency Response of the Loop Filter from a Spectrum Analyzer.

3. **Computer Simulations**

To obtain a computer simulation of the PLL, the equations obtained in section B and C were used. When the numeric values are used, the following transfer and error functions are obtained. First, the phase detector sensitivity is given as

$$K_1 = \frac{2 \times 6.5}{\pi} = 4.138 \text{ V/rad}$$

$$K_2 = 5.1$$

$$K_3 = 24.46 \times 10^3 \text{ Hz/V} \quad \text{(From Figure 3.13)}$$

$$K_3 = 24.46 \times 10^3 2\pi = 15.37 \times 10^4 \text{ rad/V}$$

$$K = K_1 K_2 K_3$$

$$K = 3.243 \times 10^6$$

To obtain the natural angular frequency, w_n, and damping factor, ζ, Equation 3.30 and Equation 3.31 are used.

$$w_n^2 = \frac{K}{\tau_1}$$

$w_n = 31208.75$ rad sec

$w_n = 4.967$ KHz.

$$2\zeta w_n = \frac{1 + K\tau_2}{\tau_1}$$

$\zeta = 0.52$

The transfer function in Equation 3.33 becomes

$$H(s) = 32156.8 \frac{s + 30288.65}{s^2 + 32457.1 + 973986070} \tag{3.45}$$

The error function in Equation 3.34 becomes

$$1 - H(s) = \frac{s^2 + 300.3s}{s^2 + 32457.1 + 973986070} \tag{3.46}$$

The Bode plot of the transfer function is given in Figure 3.18, and the Bode plot of the error function is given in Figure 3.19. It can be said that the transfer and the error function makes the phase locked loop a bandpass device, [Ref. 7].

The phase step response of the transfer function is given in Figure 3.20, using Equation 3.45. The phase step response of the error function is given in Figure 3.21, using Equation 3.46.

The frequency step response of the error function is given in Figure 3.22, using Equation 3.42. In the last three graphs, the y axis is normalized by the amount of the step function, θ radians for the phase step, and the Δw rad sec for the frequency step function.

As an experiment, a frequency shift key, FSK, modulated signal was applied to the PLL. The frequencies used were 20KHz. and 30KHz., representing the logic levels 0, 1 respectively. The oscillator outputs are given in Figure 3.23. This figure agrees well with Figure 3.20, regarding the amount of overshoot and the settling time of the VCO control signal.

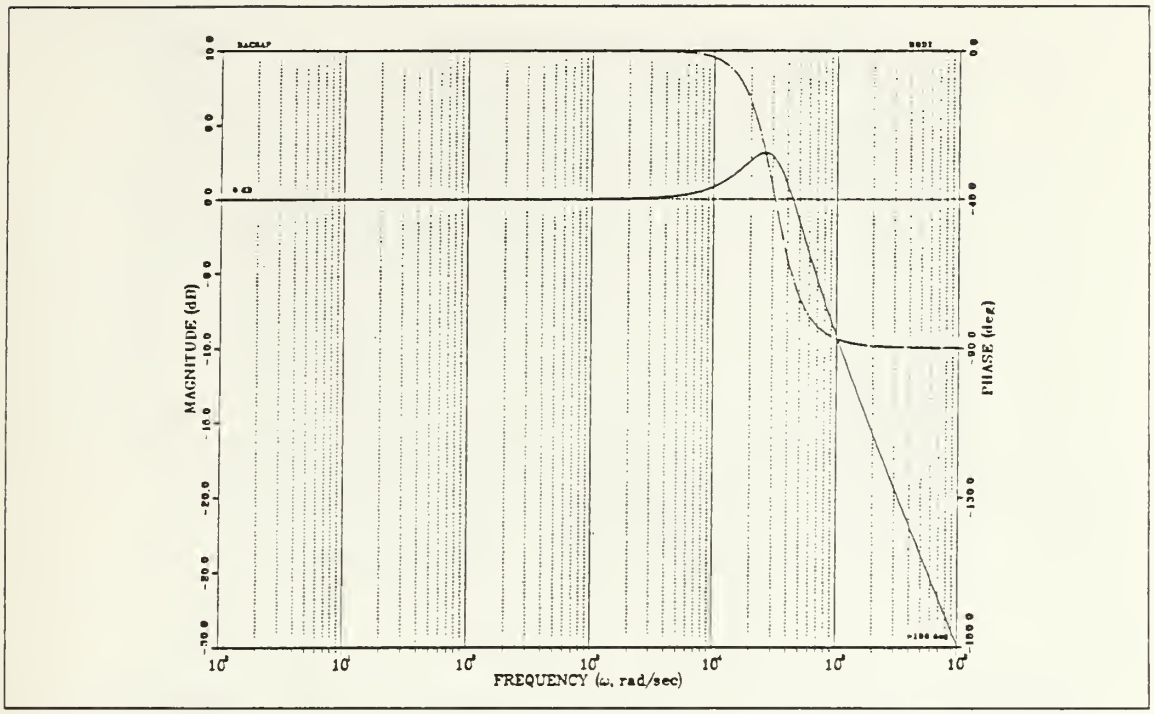

Figure 3.18 The Bode Plot of the Transfer Function.

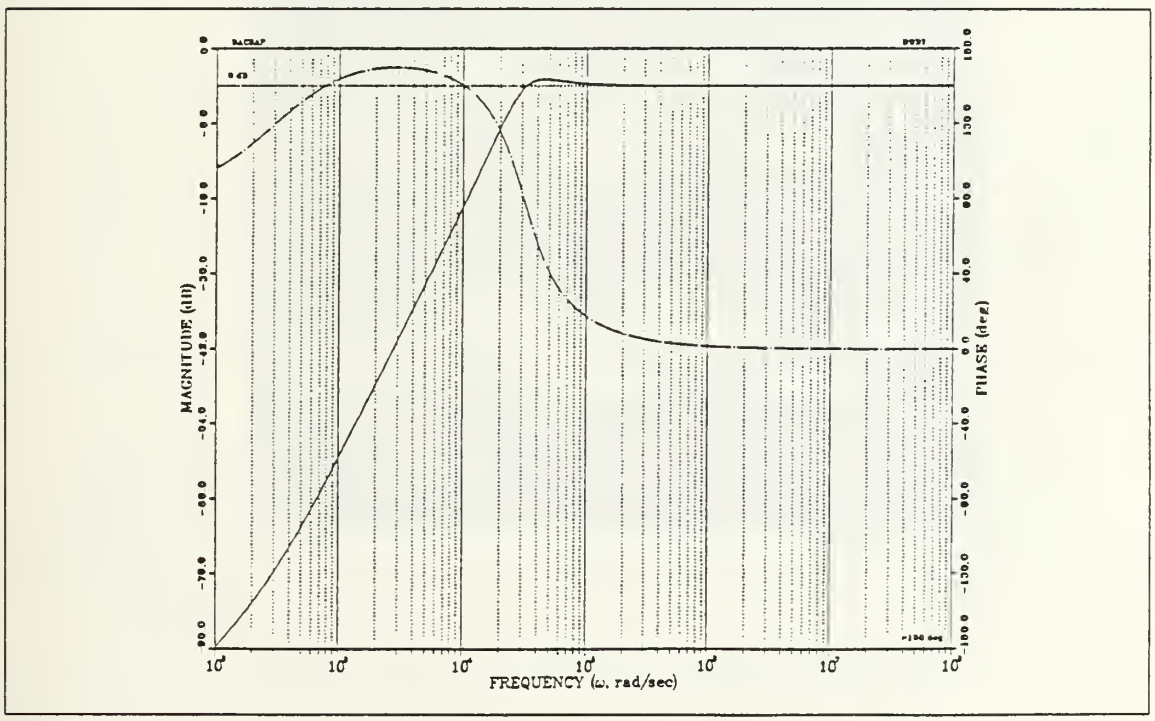

Figure 3.19 The Bode Plot of the Error Function.

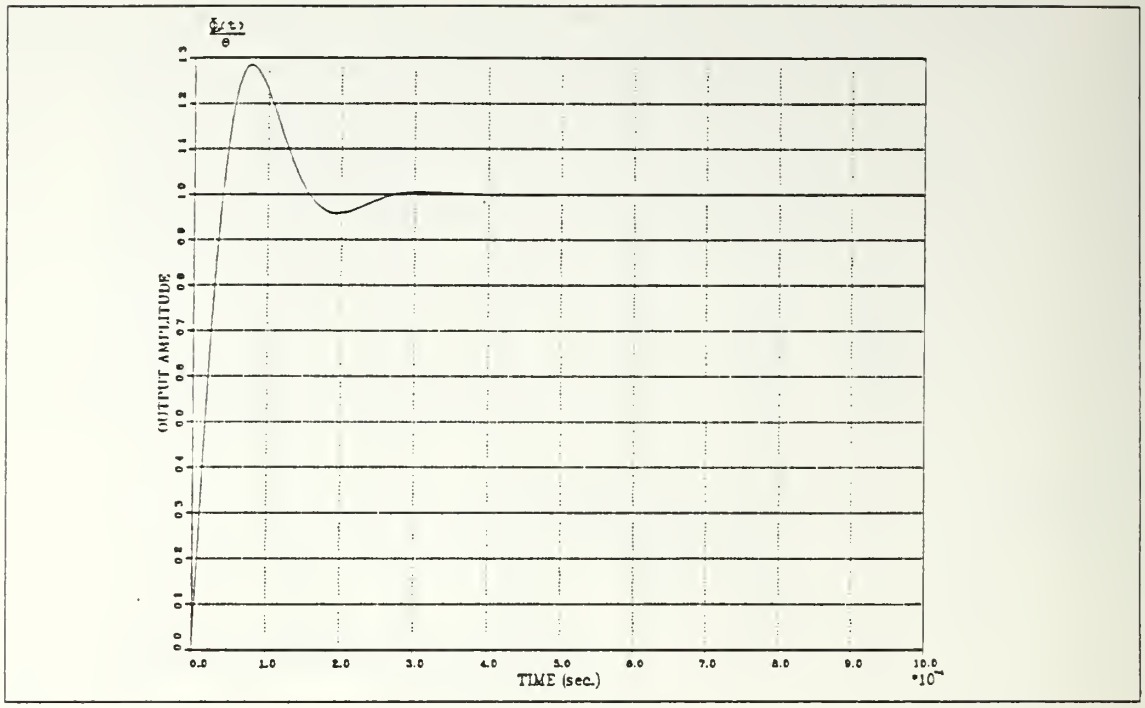

Figure 3.20 The Phase Step Response of the Transfer Function.

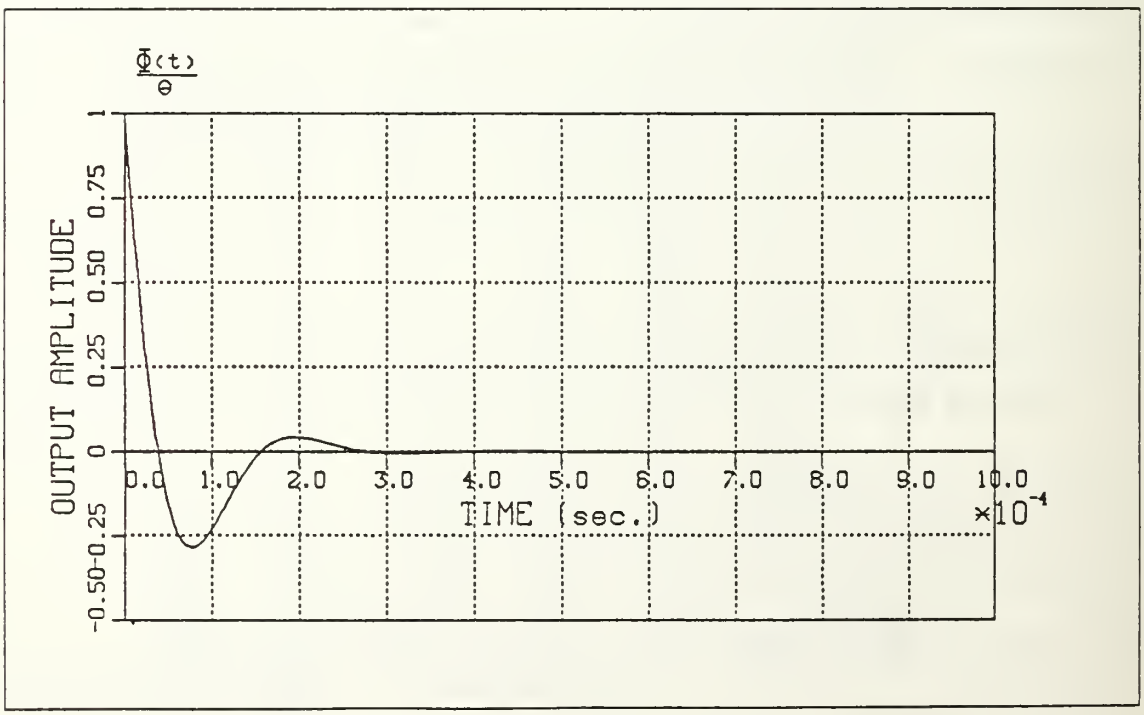

Figure 3.21 The Phase Step Response of the Error Function.

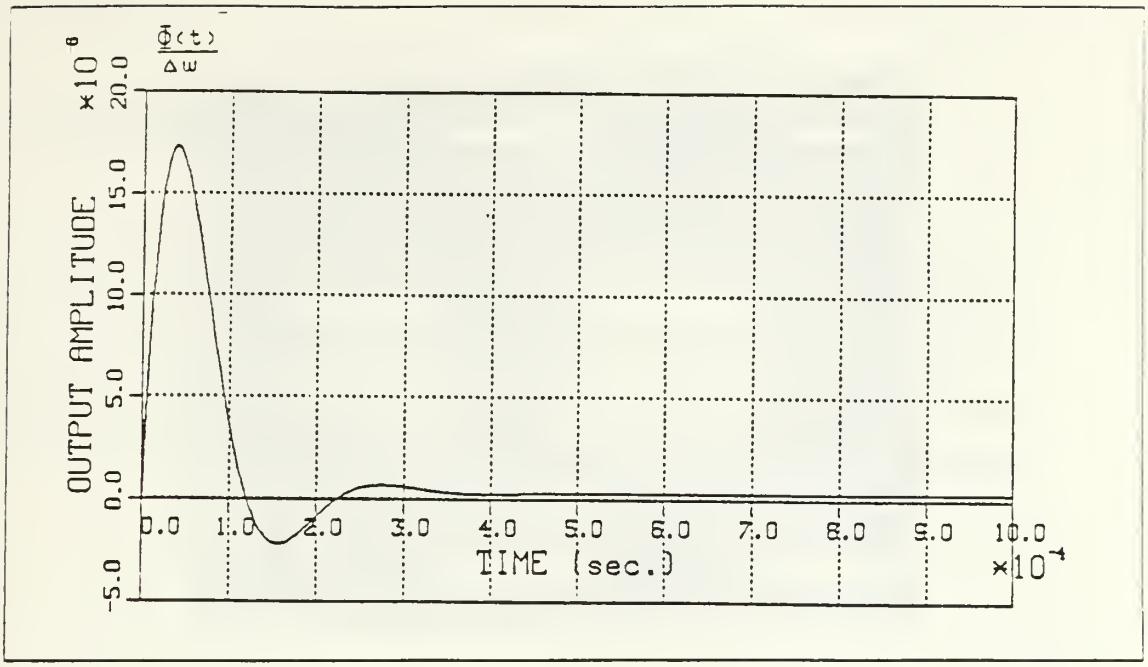

Figure 3.22 The Frequency Step Response of the Error Function.

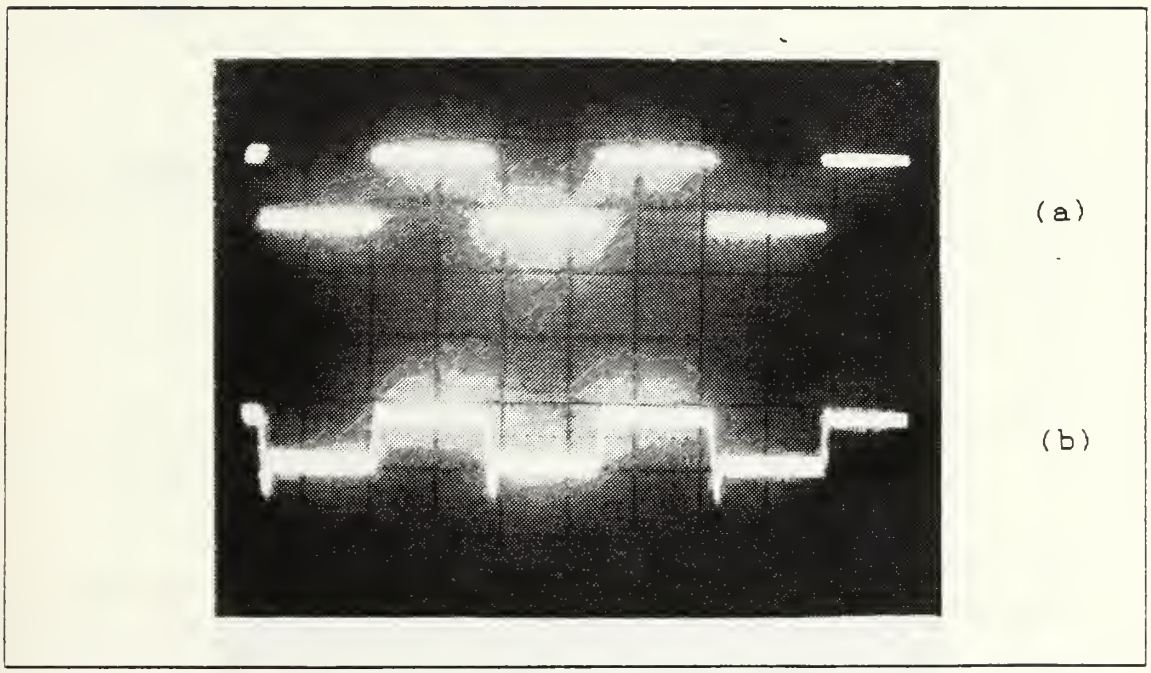

Figure 3.23 (a) The Information Signal f_i = 300 Hz.
(b) The Output of the PLL (0.5 Volt/div., 1msec/div).

IV. SWITCHED-CAPACITOR REALIZATION OF PLL

A. TWO PHASE CLOCK

The clock circuits are perhaps the most important part of an analog sampled data system. They should not be overlapping and should have a duty cycle as large as possible to permit charge transfer. A circuit that supplies nonoverlapping clocks from a single input is shown in Figure 4.1(a), and the waveforms obtained from an oscilloscope are shown in Figure 4.1(b) and (c). The clock frequency can vary as the square wave input changes.

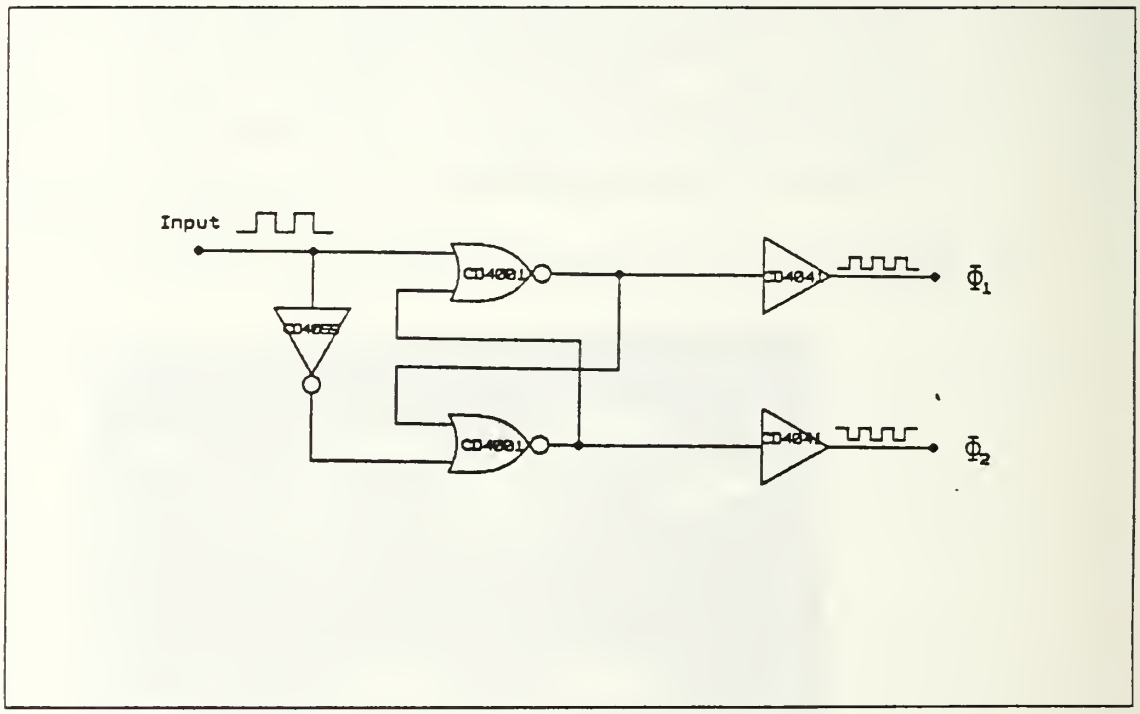

Figure 4.1 (a) Clock Circuitry.

To prevent the overloading, two digital CMOS buffers were used. The other clock circuitry components were CMOS inverters, CD4069, and CMOS NOR gates, CD4001.

B. VOLTAGE CONTROLLED OSCILLATOR (VCO)

The analog version of the VCO of Figure 3.12 was converted to switched capacitor VCO by using the bilinear SC realization in Figure 1.6. Two of the

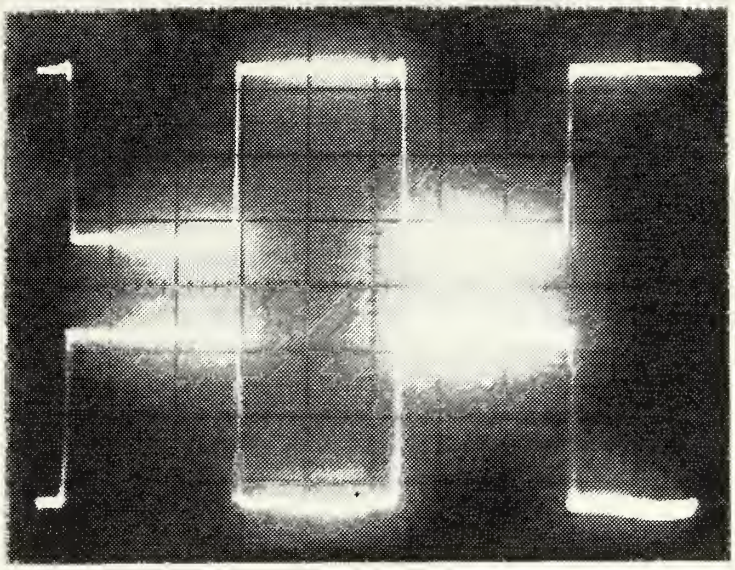

Figure 4.1 (b) Output Waveforms f_c = 200 KHz. (5 Volt div., 1 μsec div.).

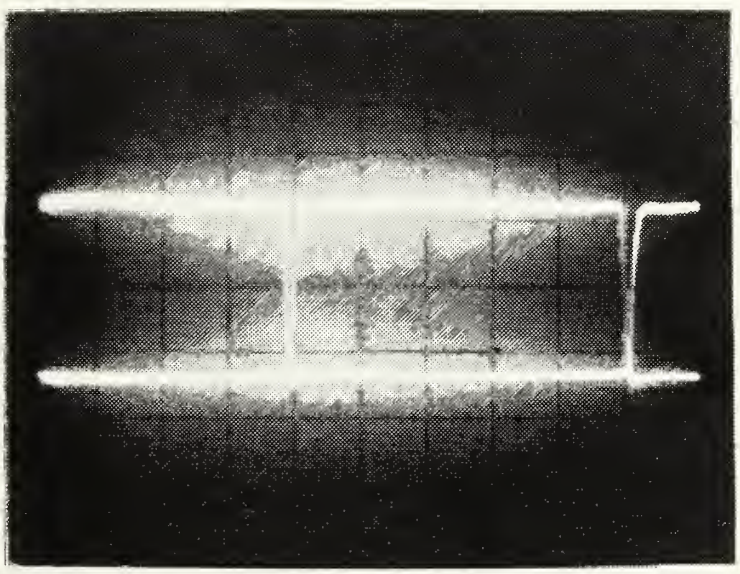

Figure 4.1 (c) Nonoverlapping Property (5 Volt div., 0.5 μsec div.).

continuous resistors were excluded to change the frequency-voltage characteristic of the VCO, R and R 2 in Figure 3.2. Since the rest of the resistors are part of the voltage dividers, as the clock frequency changes, the VCO output frequency remained constant. The major problem encountered during the experiment was the distortion of the waveforms at the higher frequencies because of the fact that the clock frequency should be an integer multiple of the oscillation frequency, [Ref. 8]. Therefore, it is important to keep the sampling rate rather high in order to minimize the phase jitter. In order to find the capacitor values for the bilinear realization, Equation 1.22 is used. The clock frequency was 200 KHz., and the calculations were made using this value. The SC version of the VCO is shown in Figure 4.2 and the waveforms are shown in Figure 4.3 and Figure 4.4 for different sampling rates. These waveforms agree well with the waveforms in Figure 3.14. The experimental frequency-voltage relationship is given in Figure 4.5 for f_c = 400 KHz. The dotted line stands for the theoretical curve whose equation is given in Equation 3.9, using $v_{31} - v_{30}$ = 1.8 Volt, obtained from Figure 4.3.

C. LOOP FILTER

1. Switched Capacitor Realization.

The SC version of the loop filter is shown in Figure 4.6. The bilinear switched capacitor realization was used for the SC conversion. This choice was made based on the results given in Chapter II. Since the best realization obtained from Chapter II was bilinear SC realization, the continuous resistors were converted to their bilinear switched capacitor equivalents. The transfer function in the s domain is given by Equation 3.15. If the bilinear transformation is applied to Equation 3.15, the transfer function in the z domain can be obtained as

$$F(s) = \xrightarrow[s=\frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)]{} F(z) = \frac{(1+\frac{2\tau_2}{T})z+(1-\frac{2\tau_2}{T})}{(1+\frac{2\tau_1}{T})z+(1-\frac{2\tau_1}{T})} \qquad (4.1)$$

Since the actual clock perod is really $T_c/2$ rather than T because the input signal is sampled twice in a single clock period, the transfer function in z domain becomes

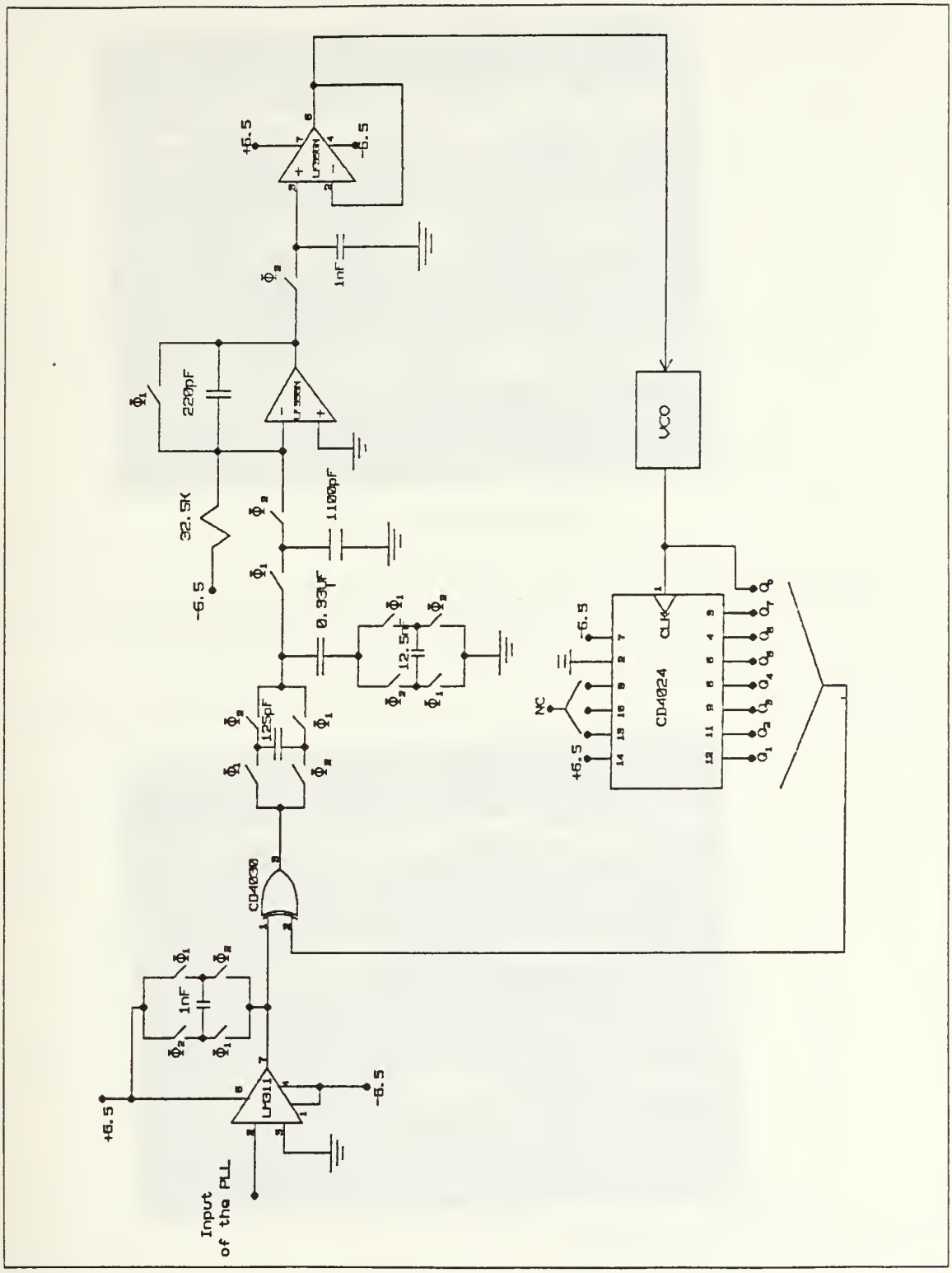

Figure 4.2 The Prototype Switched Capacitor VCO.

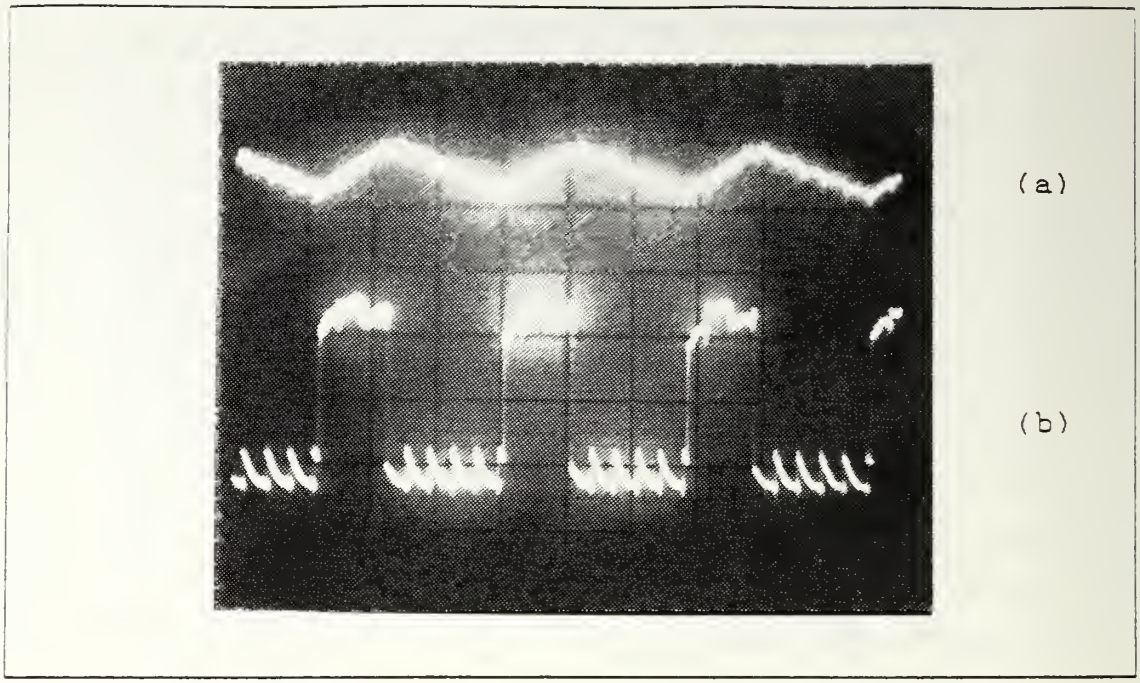

Figure 4.3 (a) The Output of the Integrator (2 Volt/div.)
(b) The Output of the VCO, f_c = 288 KHz., f_{vco} = 72 KHz. (5 Volt/div., 5 µsec/div.).

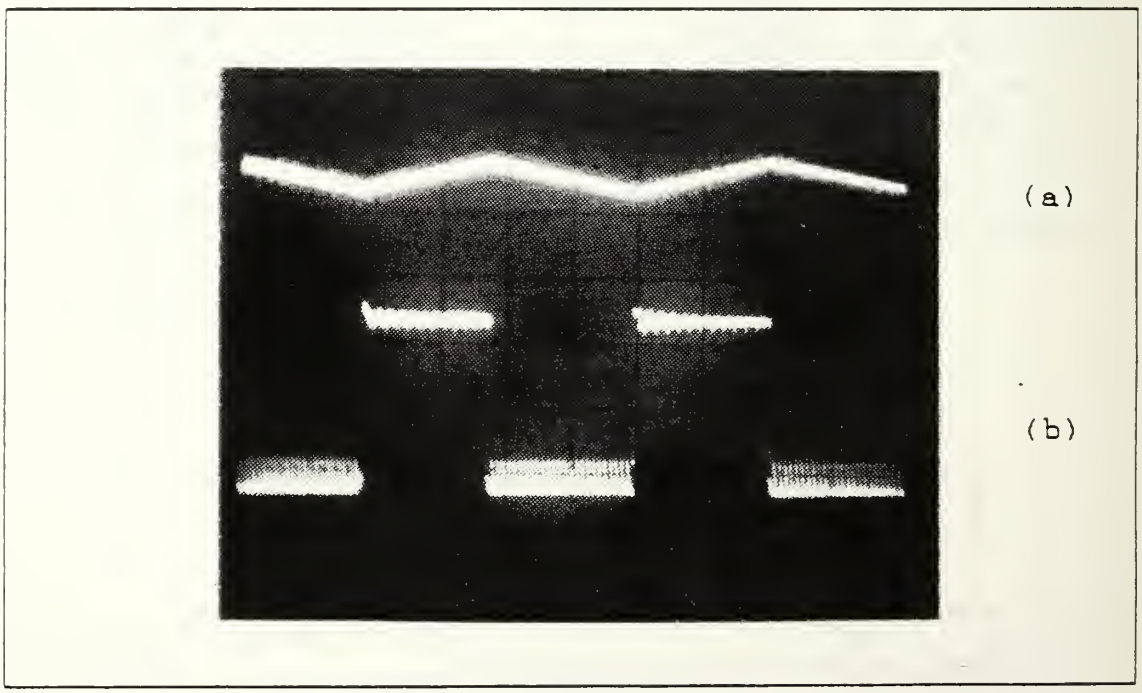

Figure 4.4 (a) The Output of the Integrator (2 Volt/div.)
(b) The Output of the VCO, f_c = 288 KHz., f_{vco} = 11.5 KHz. (5 Volt/div., 5 µsec/div.).

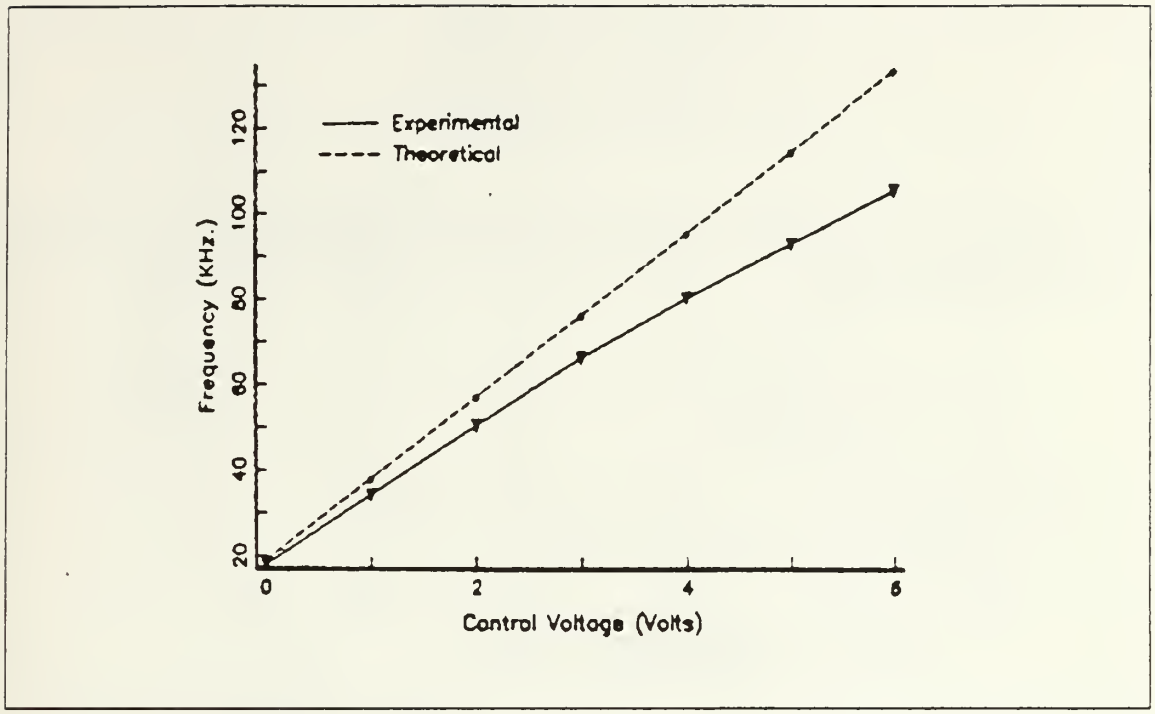

Figure 4.5 SC VCO Frequency-Voltage Relationship.

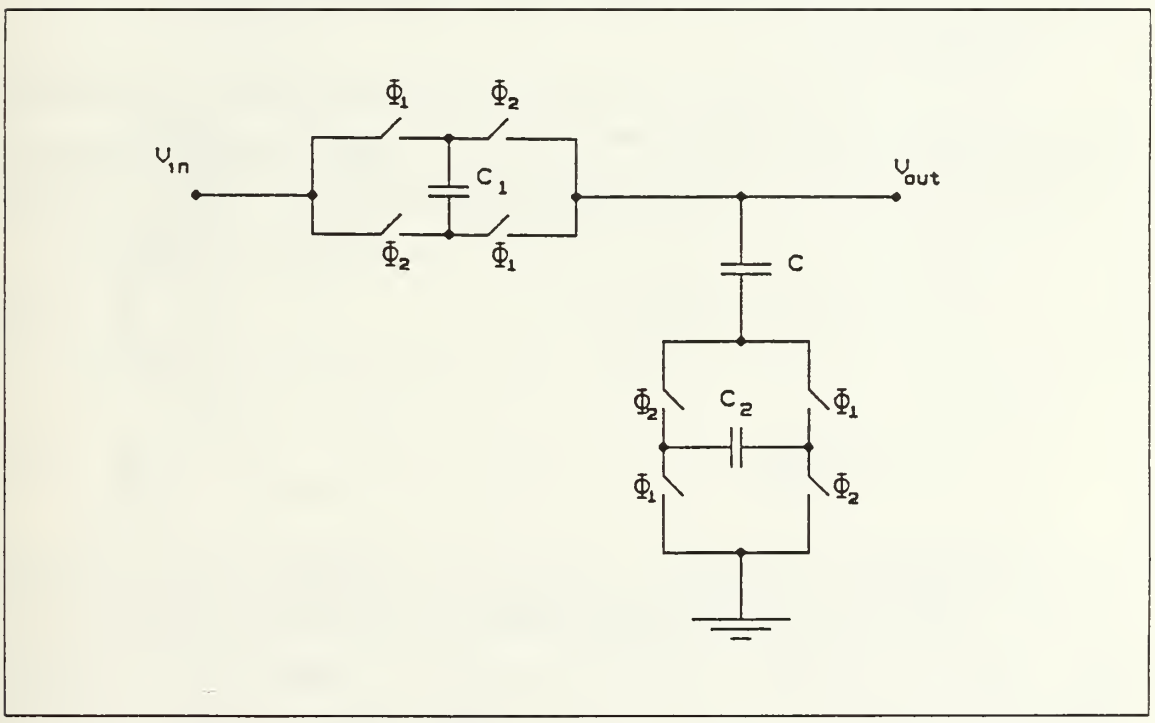

Figure 4.6 SC Realization of the Loop Filter.

$$F(z) = \frac{(1+\frac{4\tau_2}{T_c})z+(1-\frac{4\tau_2}{T_c})}{(1+\frac{4\tau_1}{T_c})z+(1-\frac{4\tau_1}{T_c})} \qquad (4.2)$$

If F(z) is to be calculated in terms of the actual experimental values, the following results can be obtained.

τ_1 = 3.33 msec.
τ_2 = 33 μsec.
f_c = 200 KHz.

and the transfer function becomes

$$F(z) = \frac{27.4z-25.4}{2665z-2663} \qquad (4.3)$$

Since the sampling rate was very high, it was not necessary to make frequency prewarping. The frequency response of this transfer function is given in Figure 4.7. This figure agrees well with the frequency response given in Figure 3.16.

2. **Loop Behavior**

The clock effect on the loop filter frequency response has a great influence on the loop behavior of the phase locked loop. Since the continuous resistances were replaced with their SC equivalent realizations, the constants of the filter, τ_1, τ_2, become

$$\tau_1 = (\frac{1}{4C_1f_c}+\frac{1}{4C_2f_c})C \qquad (4.4)$$

$$\tau_2 = \frac{C}{4C_2f_c} \qquad (4.5)$$

In the experiment C_1 = 125 pF, C_2 = 12.5 nF, C = 0.33 μF, and f_c = 200 KHz. The capacitor values were found by using Equation 1.22. The time constants were τ_1 = 33 μsec, and τ_2 = 3.33 μsec. If the clock frequency is changed, these time constants change. If the clock frequency is increased, τ_1 and τ_2 decreases linearly. For f_c = 300 KHz. τ_2 = 22 μsec, and the pole and zero frequencies are calculated as

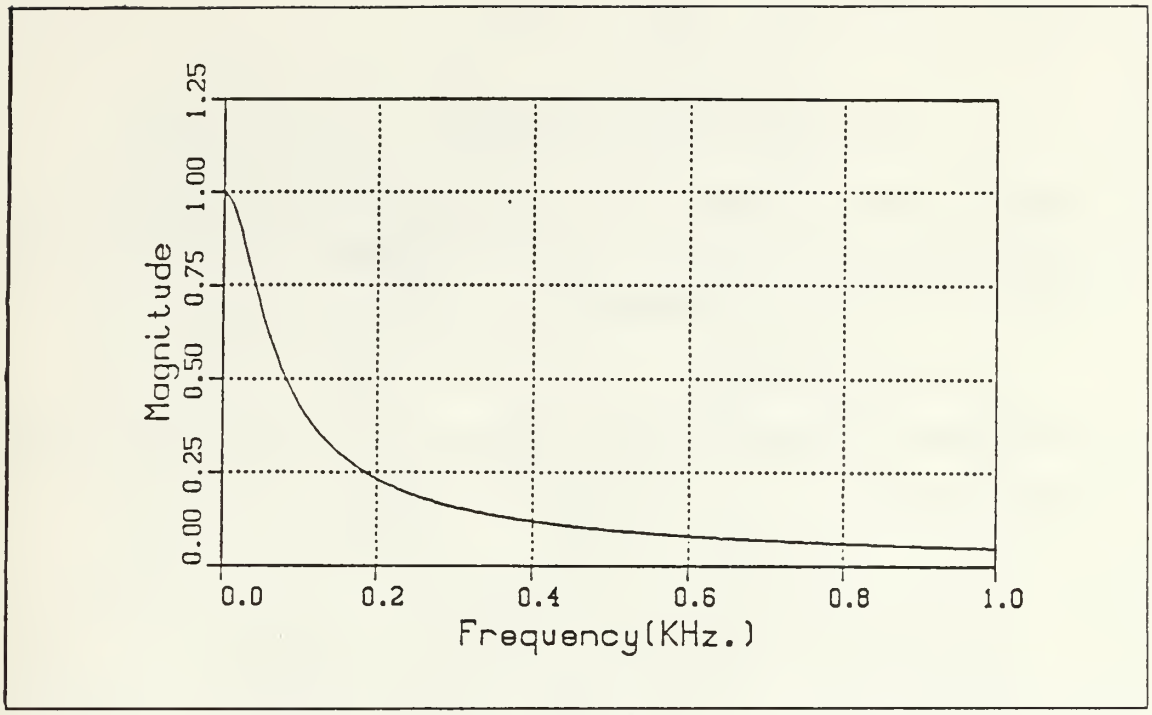

Figure 4.7 (a) The Magnitude Response of Equation 4.3.

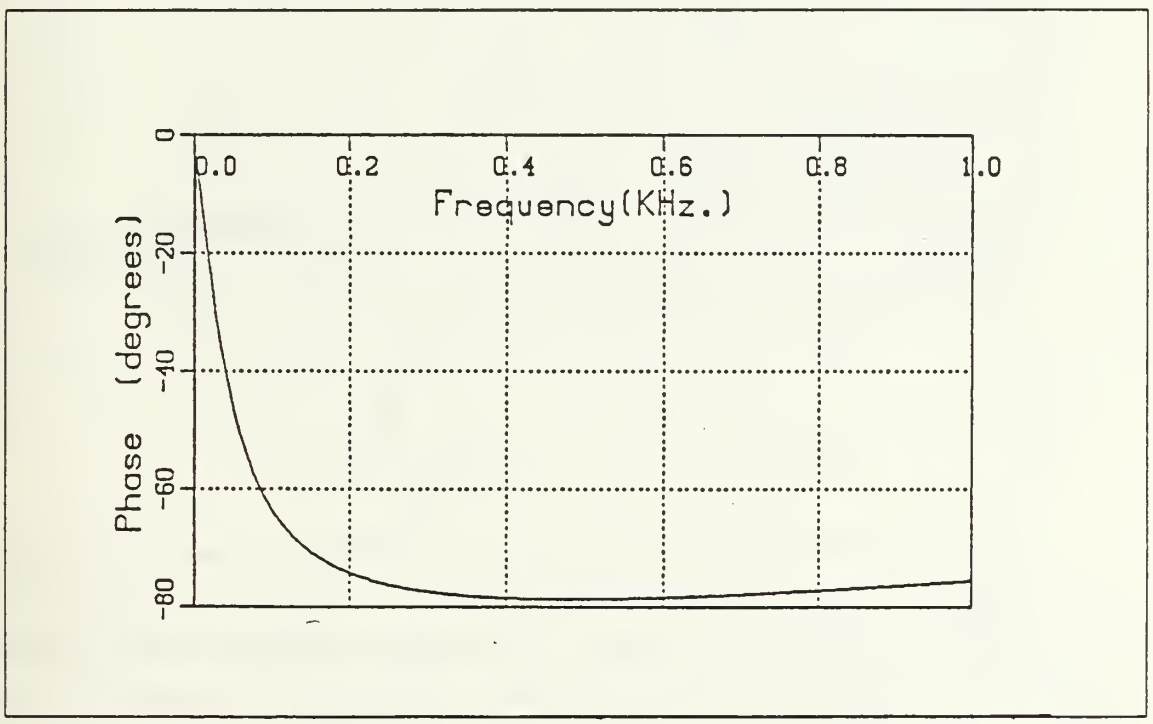

Figure 4.7 (b) The Phase Response of Equation 4.3.

$$f_1 = \frac{w_1}{2\pi} = \frac{1}{2\pi\tau_1} = 71.7 \text{ Hz.}$$

$$f_2 = \frac{w_2}{2\pi} = \frac{1}{2\pi\tau_2} = 7.23 \text{ KHz.}$$

From these results it can be seen that if the clock frequency is increased by 50%, the critical frequencies increase 50%. For f_c = 400 KHz. τ_1 = 1.665 μsec. τ_2 = 16.5 μsec, and the pole and zero frequencies

f_1 = 96 Hz.

f_2 = 9.6 KHz.

The clock effect is shown in Figure 4.8. The results were obtained from a digital signal processor, SD-360.

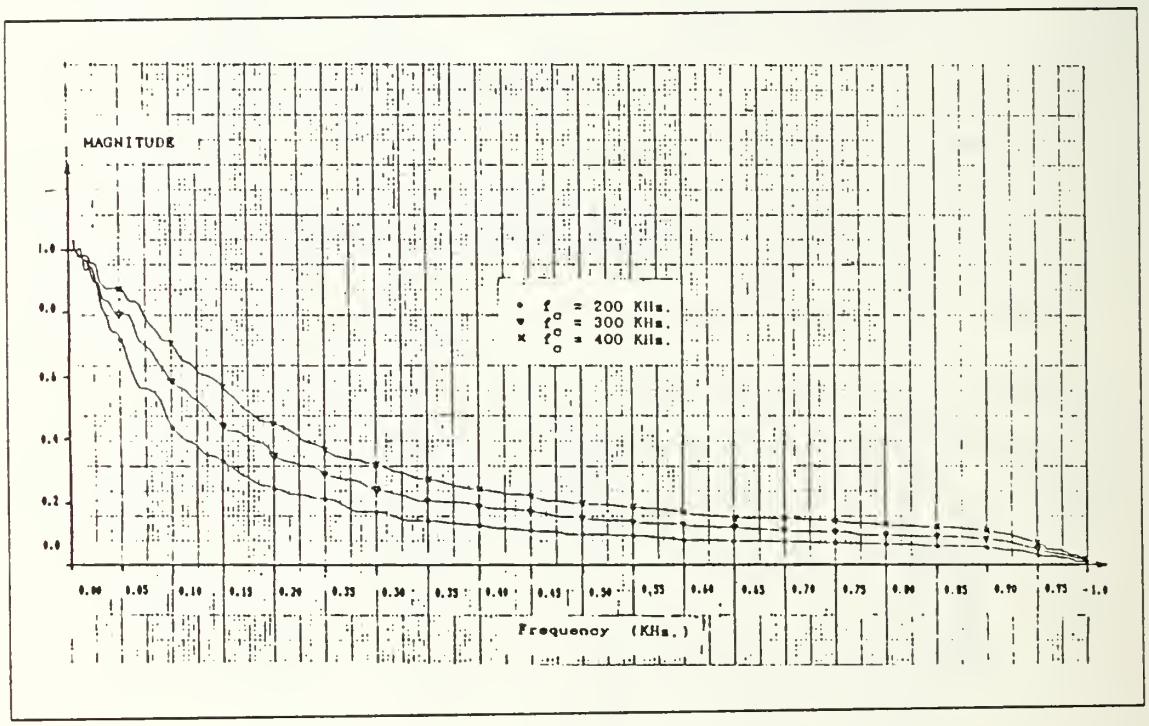

Figure 4.8 The Clock Effect on the Loop Filter.

The SC version of the phase locked loop is shown in Figure 4.9. This circuit was obtained by substituting the continuous resistors of Figure 3.15 with their bilinear SC realizations. The circuit of Figure 4.2 was used as the SC voltage controlled oscillator. The picture in Figure 4.10 was taken while the PLL was in lock, f_c = 200 KHz., f_{vco} = 20 KHz.

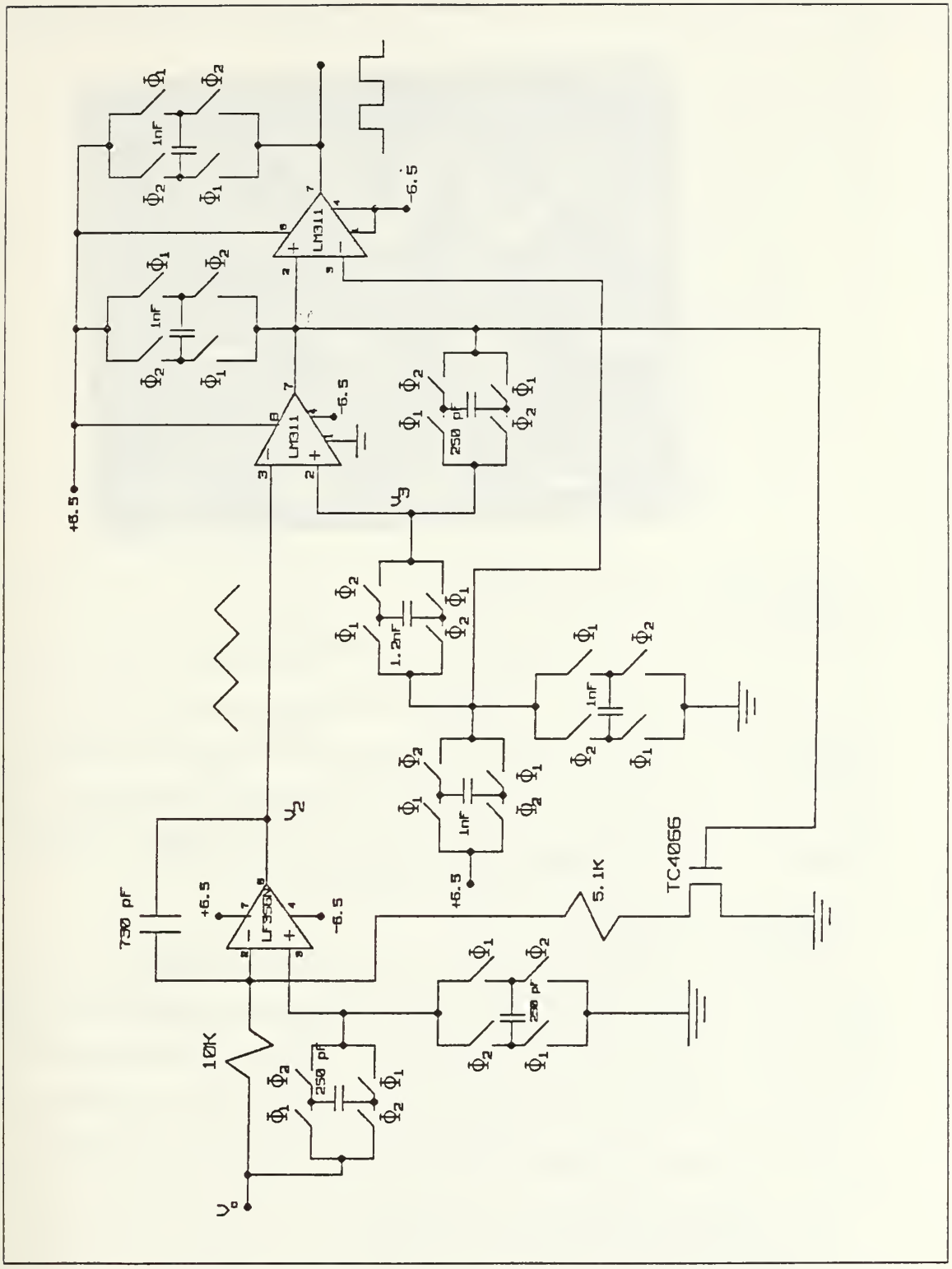

Figure 4.9 The SC Version of the PLL.

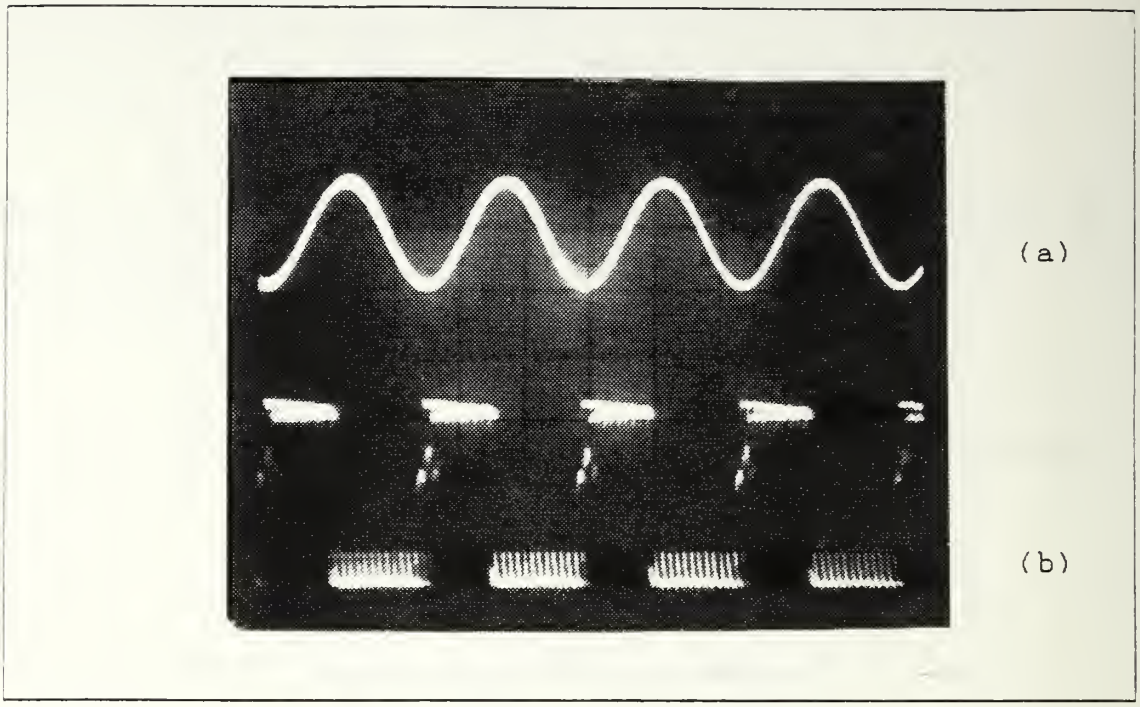

Figure 4.10 (a) The Input to the PLL (b) The Output of the SC VCO (5 Volt/div., 20 μsec/d

Referring to Figure 1.8, the capture and lock ranges were recorded for various clock frequencies. Since the number of meeting points of the VCO frequency and the clock frequency decreased as the sampling rate decreased, it was difficult to measure the capture and lock ranges accurately for higher input frequencies. The capture and lock ranges were recorded between 2.4 KHz. and 64 KHz.

D. LOOP AMPLIFIER

For the SC realization of the loop amplifier shown in Figure 3.9 the circuit shown in Figure 4.11 was used. The acquisition voltage was supplied from the negative power supply to obtain a free running frequency at 25 KHz.. For this purpose the 18 KΩ resistor in Figure 3.15 was replaced with a 32.5 KΩ resistor. To change the free-running frequency externally this resistance was not replaced by a SC realization. The free-running frequency was made lower than the analog prototype PLL free-running frequency to make the sampling rate rather high.

As an application, the resistor R of Figure 3.9 was replaced by the parallel SC resistor realization and R_f was replaced by a modified series SC resistor realization. The series switch of this series SC resistor realization was removed because it was not

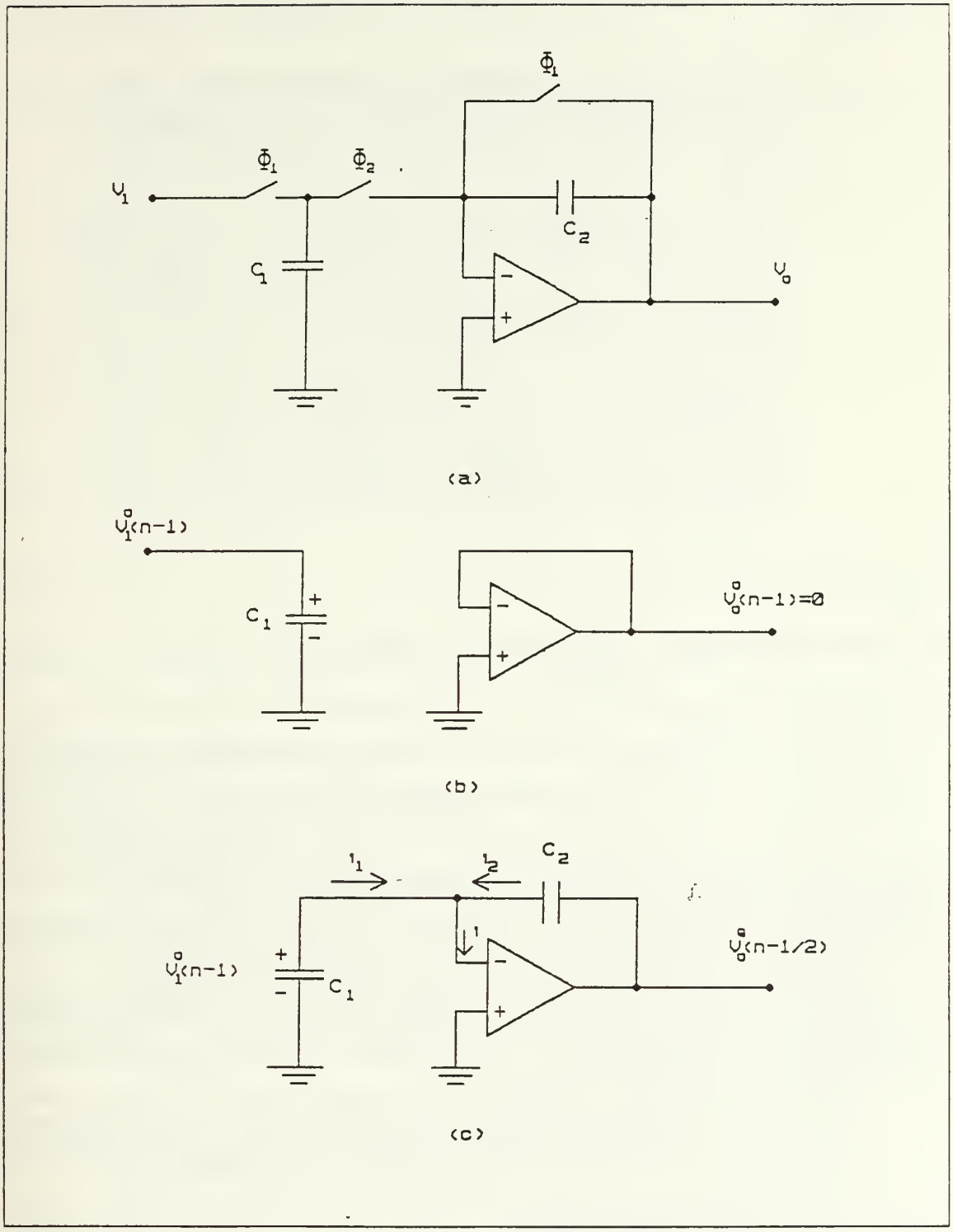

Figure 4.11 (a) A Practical Realization of Figure 3.9
(b) Equivalent Circuit of (a) when Φ_1 is closed
(c) when Φ_2 is closed.

necessary and would cause the op amp to have no feedback during one of the phase periods.

If the charge conservation approach is used to analyze Figure 4.11(b), the components of Equation 2.18 are identified for the even clock phase period.

$$(n\text{-}1\ 2) \le t\ T < n$$

$$q_L^{\,e}(t') = q_m^{\,o}(t) + q_c^{\,o,e}(t) \qquad t' > t$$

$$q_L^{\,e}(n\text{-}1\ 2) = C_2 v_o^{\,e}(n\text{-}1\ 2) \tag{4.6}$$

$$q_m^{\,o}(n\text{-}1) = 0$$

$$q_c^{\,o}(n\text{-}1) = -\,C_1 v_1^{\,o}(n\text{-}1) \tag{4.7}$$

$$v_o^{\,e}(n\text{-}1\ 2) = -\,(C_1\ C_2) v_1^{\,o}(n\text{-}1) \tag{4.8}$$

$$H^{oe}(z) = \frac{V_o^{\,e}(z)}{V_1^{\,o}(z)} = -\,\frac{C_1}{C_2}\, z^{-1\ 2} \tag{4.9}$$

It can be seen that Figure 4.11 acts like an inverting amplifier with a gain of $C_1\ C_2$ and a delay of T 2 seconds. Note that voltage gain can be achieved if C_1 is larger than C_2. It is also noted that at no time the op amp was without some form of feedback. In the even phase period, C_2 is charged to the voltage given by Equation 4.8 and will hold that voltage indefinitely under ideal conditions. Therefore, as long as $v_1^{\,o}(n\text{-}1)$ does not cause $v_o^{\,e}(n\text{-}1\ 2)$ to saturate the op amp, the circuit performs as expected.

It is observed that the z-domain transfer function is multiplied by a half-delay, $z^{-1\ 2}$. This $z^{-1\ 2}$ can be changed to a full delay, z^{-1}, by the use of a sample-and-hold circuit. The circuit is given in Figure 4.12.

Here it is seen that during the Φ_2 phase $v_o(n)$ is stored in the holding capacitor C_h. During the next phase period, when Φ_1 closes, $v_o(n)$ is available at v_{oh}. Therefore

$$v_{oh}^{\,o}(n+1\ 2) = v_o^{\,e}(n) \tag{4.10}$$

$$V_{oh}^{\,o}(z) = V_o^{\,e}(z) z^{-1\ 2} = -\,(C_1\ C_2) z^{-1} V_1^{\,o}(z) \tag{4.11}$$

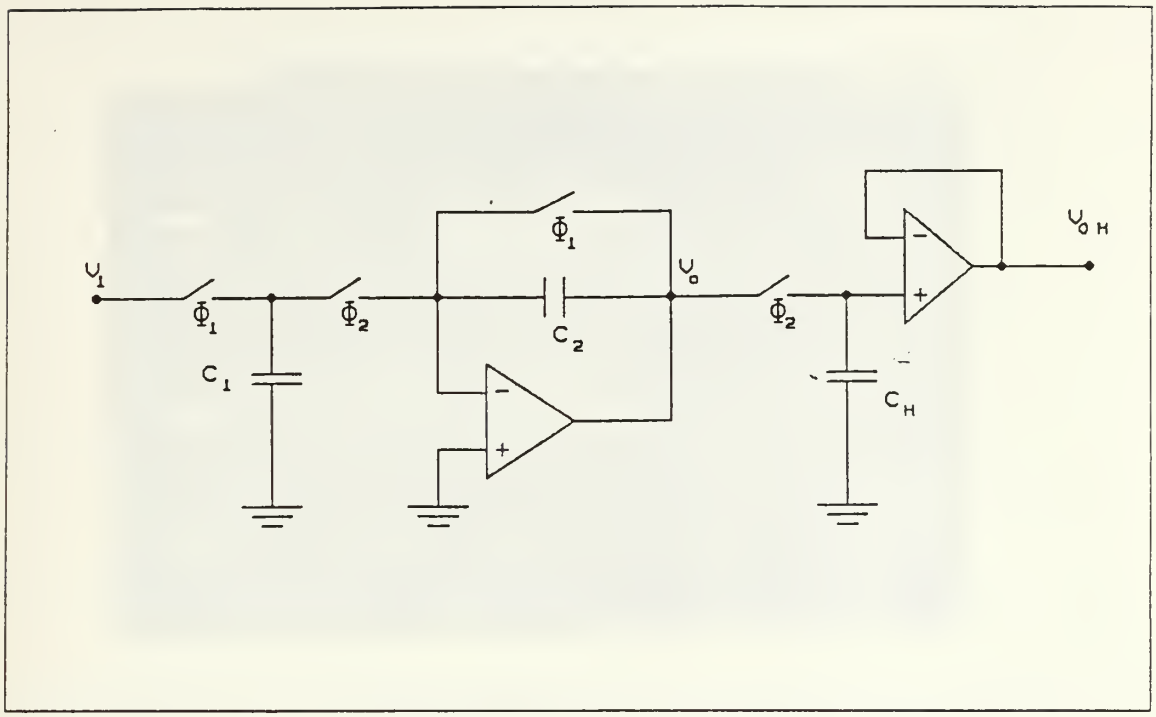

Figure 4.12 Use of the Sample-and-hold to Obtain an Inverting Amplifier with a Full Delay.

To show these delays and the waveforms of v_o and v_{oh}, the picture in Figure 4.13 was taken from an oscilloscope.

E. APPLICATIONS OF THE SC PLL

1. FSK Demodulator

The frequency shift-keying (FSK) is used for transmitting low and medium speed digital data over existing telephone lines. An FSK modulator encodes the digital data into an audio-frequency signal, where the two binary states are represented by two discrete frequencies. The FSK demodulator demodulates the received FSK signal and restores the original data in a binary format. The phase-locked loop techniques are widely used for FSK demodulation. When the PLL is locked on the FSK signal, the PLL output voltage tracks the shifts in the input frequency.

The demodulator was breadboarded using the SC phase locked loop. The clock frequency was 300 KHz. The discrete frequencies were f_1 = 20 KHz. and f_2 = 30 KHz.. The maximum FSK transmission rate was recorded as 1200 baud. A picture of a transmission at 300 baud is shown in Figure 4.14. The output of the PLL was passed through a low-pass filter with a pole frequency of 1.33 KHz., and fed to a comparator to obtained the desired logic levels.

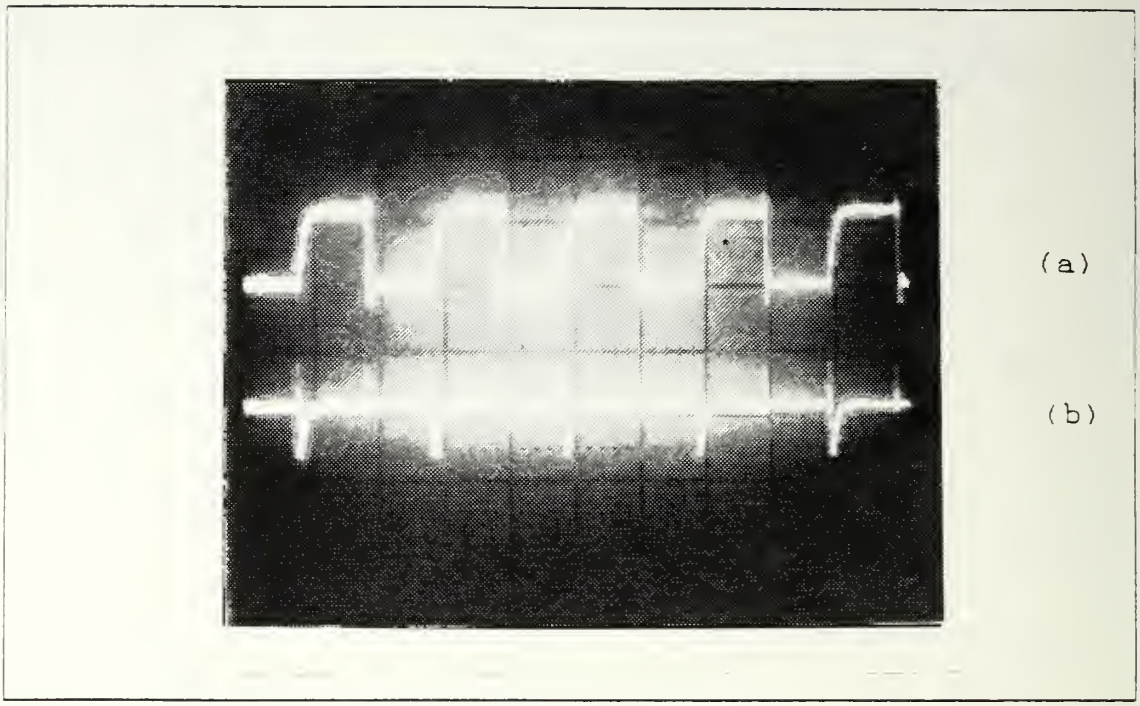

Figure 4.13 (a) Output of the Inverting Amplifier with a Half Delay
(b) Output of the Sample-and-hold with a Full Delay (f_c = 250 KHz., 2 Volts div., 2 μsec div.)

2. Frequency Synthesis

A frequency synthesizer can be built around a PLL as shown in Figure 4.15, a frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o while the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. A digital counter, CD4024, was used as the frequency divider shown in Figure 4.9. If Q_4, pin 6 of the counter, is used as an input to the phase comparator, the comparator input frequency will be a divide-by-16 from that of the VCO output frequency. This will result in a VCO output of 16 times the input frequency as long as the loop remains in lock.

Using the configuration in Figure 4.15, frequencies lower than the input signal frequency can also be obtained by using the other outputs of the counter. If Q_1 is used as the input to the phase comparator the input frequency is divided by 2 at the Q_2 output, by 4 at the Q_3 output, by 8 at the Q_4 output, and so on.

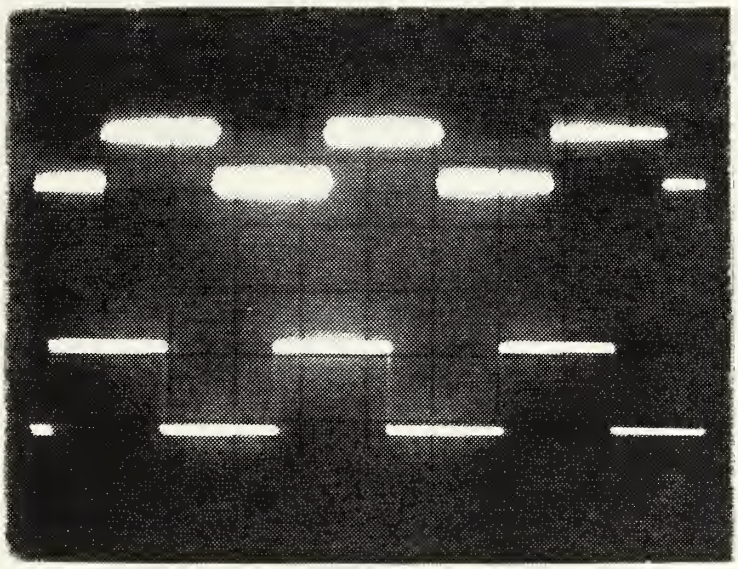

Figure 4.14 (a) Binary Data Input to be Modulated
(b) Demodulated Binary Data (5 Volts/div., 1 msec/div.).

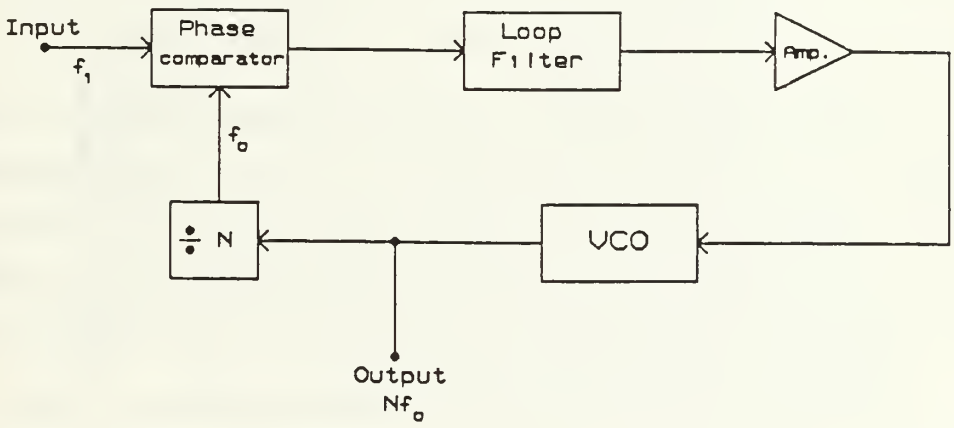

Figure 4.15 Frequency Synthesizer Block Diagram.

3. Tracking Filter

SC filters have pole frequencies which are directly proportional to the clocking frequency. It follows that the frequency response of a SC filter can be frequency scaled by programming the frequency of the clock in the desired manner. This property is used in the design of the tracking filter show in Figure 4.16, [Ref. 9].

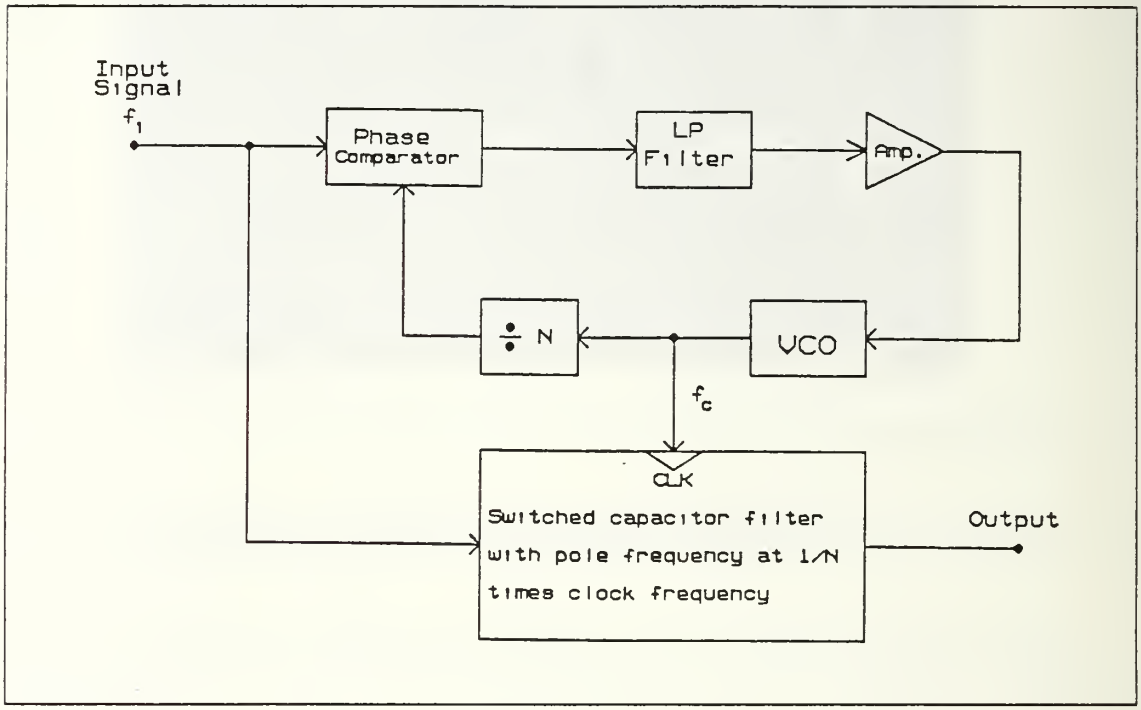

Figure 4.16 Block Diagram of a Tracking Filter.

The input signal is fed both to a phase-locked loop as well as to the SC filter. When the PLL locks onto the input signal, the VCO frequency will be exactly N times the input frequency. The VCO output is used to drive the switches of the filter which is designed to have a pole frequency equal to (1/N) times the clocking frequency. It follows that the pole frequency of the filter will be equal to the frequency of the input signal, provided that the phase-locked loop is in lock.

The switched capacitor filter can be designed to have any desired function (e.g., bandpass, low pass, etc.) as well as any desired order. A discrete prototype of the circuit of Figure 4.16 was built and the PLL circuit of Figure 3.15 was used in Figure 4.17. The divide-by-N circuit was chosen as a divide-by-16 by using the Q_4, output of the binary counter, CD4024.

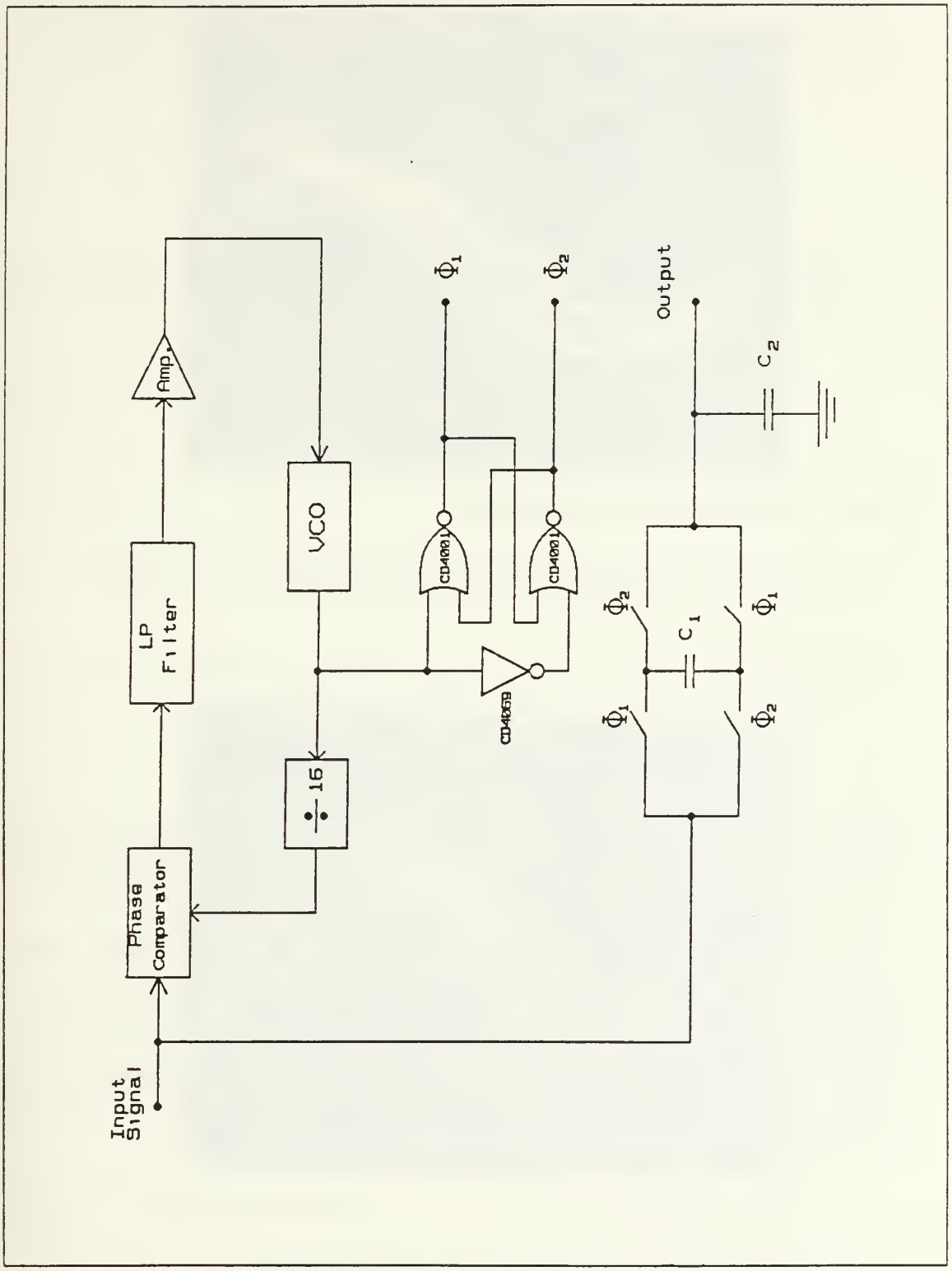

Figure 4.17 The Prototype Low-Pass Tracking Filter.

A first order SC low-pass filter was constructed using the bilinear SC realization. From Equation 2.1 the pole frequency is given $w_1 = 1\,\tau_1 = 1\,R_1C_2$ rad sec.

$$f_1 = \frac{1}{2\pi R_1 C_2} \text{ Hz.} \tag{4.12}$$

If the bilinear SC realization is used for the continuous resistor, R_1, the pole frequency f_i becomes

$$f_1 = \frac{2f_c}{\pi}\frac{C_1}{C_2} \tag{4.13}$$

Since $f_c = 16\,f_i$, Equation 4.13 becomes

$$f_1 = \frac{32}{\pi} f_i \frac{C_1}{C_2}$$

$$\frac{C_1}{C_2} = \frac{\pi}{32}$$

provided that $f_1 = f_i$. If the PLL is in lock, one can always obtain pole frequency attenuation of $1\ \sqrt{2}$ and a phase shift of 45 degrees at the filter output since a first order low-pass filter is used.

In the experiment $C_1 = 1$ nF, and $C_2 = 10$ nF. The output phase and magnitude of the SC filter was observed to remain constant irrespective of the input frequency between 1 KHz. and 6.5 KHz. The waveforms of Figure 4.17 are shown in Figure 4.18 and Figure 4.19 for a 4 KHz. and 6.25 KHz. for sinusoidal input signal, respectively. The filter output had the same pole frequency attenuation and a 45 degree phase shift.

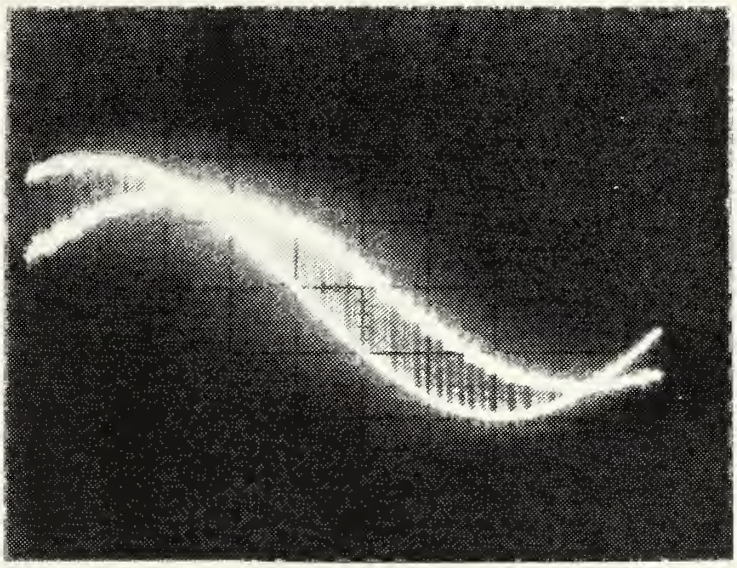

Figure 4.18 The Input and the Output Waveforms of the Figure 4.17, f_i = 3 KHz. (1 Volt/div., 20 μsec/div.).

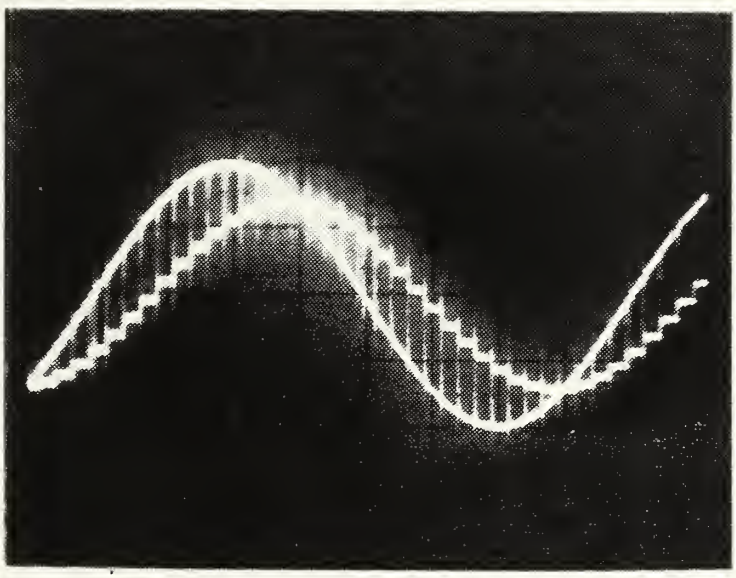

Figure 4.19 The Input and the Output waveforms of the Figure 4.17, f_i = 6.25 KHz. (1 Volt/div., 20 μsec/div.).

V. CONCLUSION

In this thesis research the resistors of an RC network were replaced by the switched capacitor (SC) networks, resulting in a sampled data equivalent network. Many of the switched capacitor networks described in the literature have been either for filtering or analog-to-digital conversion applications. SC networks are also useful for realizing many other signal processing functions. In the research some of the SC building blocks, useful in realizing adaptive systems, were described as well as some passive RC filter applications.

As stated in the abstract, it was shown that the switched capacitor resistors were exactly equivalent to resistors by themselves, however, such an equivalence might not hold true when the realizations were used to replace resistors of an RC active network due to the discrete-time nature of SC networks. It was also shown that it was technologically possible to include digital circuitry along with SC networks in the same IC network.

During the research, first, the types of realization methods and their properties were discussed. Furthermore, some of the main SC building blocks were presented such as a voltage controlled oscillator (VCO), an amplifier, and a hard limiter. These building blocks led to the design of a more complicated SC circuit, a phase-locked loop (PLL). First, an analog version of the PLL was breadboarded, then, it was converted to a switched capacitor PLL using the realization methods mentioned before.

Experiments showed that the clock frequency should be an integer multiple of the oscillation frequency. For this reason the sampling ratio was kept rather high in order to minimize the phase jitter. This was the major limitation on the SC PLL design. To avoid this restriction, the SC VCO was replaced by its analog version, resulting in a hybrid phase-locked loop, [Ref. 10]. The results obtained from the hybrid version were very close to the analog version ones. The hybrid circuit using SC network technology, also had the advantages such as accuracy, practical implementation, and lower cost. In the design mostly MOS switches, MOS amplifiers, and MOS digital circuits were used to take advantages of the MOS technology and probable further VLSI design of the circuit.

APPENDIX
A

TABLE 1
SUMMARY OF SOME Z-TRANSFORM PROPERTIES

z - TRANSFORM	SEQUENCE
$aX(z) + bV(z)$	$ax(n) + bv(n)$
$z^{-k} Y(z)$	$y(n-k)$
$Y(z/b)$	$b^n y(n)$
$-z \frac{dY(z)}{dz}$	$ny(n)$
$Y(z^{-1})$	$y(-n)$
$X(z) V(z)$	$x(n) * v(n)$

TABLE 2

RELATIONSHIPS BETWEEN CONTINUOUS AND DISCRETE DOMAINS

Transformation	$H(s) \longrightarrow H(z)$	$H(z) \longrightarrow H(s)$
Backward	$s = \frac{1 - z^{-1}}{T}$	$z = \frac{1}{1 - sT}$
Forward	$s = \frac{1}{Tz^{-1}}(1 - z^{-1})$	$z = 1 + sT$
Bilinear	$s = \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}$	$z = \frac{1 + (T/2)s}{1 - (T/2)s}$
Impulse Invariant	$s = (1/T)\ln z$	$z = e^{sT}$

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